EXHIBIT 2

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.; MICRON SEMICONDUCTOR PRODUCTS, INC.; and MICRON TECHNOLOGY TEXAS LLC,
Petitioners,

v.

NETLIST, INC.,
Patent Owner.

Case No. IPR2021-00744
U.S. Patent No. 10,489,314

PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 10,489,314

TABLE OF CONTENTS

Page

I. Introduction 1
II. Requirements for *Inter Partes* Review 2
A. The '314 Patent Is Available For *Inter Partes* Review 2
B. Grounds 2
III. The '314 Patent 3
A. Earliest Effective Filing Date 3
B. Level of Ordinary Skill in the Art 3
C. Overview of the '314 Patent 4
D. Relevant Prosecution History of the '314 Patent Family 6
IV. Claim Construction 6
V. Grounds for Unpatentability 8
A. Overview of the Prior Art 8
1. Halbert 8
2. Overview of JESD21-C 13
3. Overview of JESD79-2A 15
B. Ground 1: Halbert in View of a POSITA's knowledge Render Claims 1-2, 6, 8, and 12-14 Obvious 17
1. Claim 1 17
a. Limitation [1.1] 17
b. Limitation [1.2] 21
c. Limitation [1.3] 22
d. Limitation [1.4] 22
e. Limitation [1.5] 26
f. Limitation [1.6] 27
g. Limitation [1.7] 28
h. Limitations [1.8]-[1.9] 29
i. Limitation [1.10] 30
j. Limitation [1.11] 33

2. Claim 2 35
a. Limitation [2.1] 35
b. Limitation [2.2] 36
3. Claim 6 37
4. Claim 8 37
5. Claim 12 38
a. Limitation [12.1] 38
b. Limitation [12.2] 39
6. Claim 13 41
a. Limitation [13.1] 41
b. Limitation [13.2] 41
7. Claim 14 42
a. Limitation [14.1] 42
b. Limitation [14.2] 42
c. Limitation [14.3] 43
C. Ground 2: Halbert in View of JESD21-C Render Claims 3 and 9-10 Obvious 45
1. Claim 3 45
a. Limitations [3.1]-[3.2] 45
b. Limitations [3.3]-[3.4] 46
c. Limitations [3.5]-[3.6] 53
d. Limitations [3.7]-[3.8] 57
e. Limitation [3.9] 60
2. Claim 9 61
a. Limitation [9.1] 61
b. Limitation [9.2] 61
c. Limitations [9.3]-[9.4] 64
3. Claim 10 66
a. Limitations [10.1]-[10.2] 66
D. Ground 3: Halbert in View of JESD79-2A Render Claim 5 Obvious 66
1. Claim 5 66

a. Limitation [5.1] 66
b. Limitation [5.2] 70
c. Limitation [5.3] 71
d. Limitation [5.4] 72
e. Limitation [5.5] 74
f. Limitation [5.6] 75
E. No Secondary Considerations Exist 76
VI. The Parallel District Court Case Does Not Warrant Denying Institution.....76
VII. Discretionary Denial Under § 325(d) Is Not Warranted.....78
VIII. Mandatory Notices.....82
A. Real Parties-in-Interest.....82
B. Related Proceedings.....82
C. Lead and Backup Counsel 82
D. Electronic Service 83
IX. Fees.....83
X. Conclusion.....83

TABLE OF AUTHORITIES

Page(s)

Cases

Advanced Bionics, LLC v. MED-EL Elektromedizinische Geräte GmbH,
IPR2019-01469, Paper 6, 8 (PTAB Feb. 13, 2020).....78, 79, 80, 81

Apple Inc. v. Fintiv, Inc.,
IPR2020-00019, Paper 11 (PTAB Mar. 20, 2020).....76

Apple, Inc. v. Omni MedSci, Inc.,
IPR2020-00029, Paper 7, 8 (P.T.A.B. Apr. 22, 2020) 81

Apple, Inc. v. SEVEN Networks, LLC,
IPR2020-00156, Paper 10 (P.T.A.B. Jun. 15, 2020) 77

Micron Tech., Inc. et al. v. Unification Techs. LLC,
IPR2021-00344, Paper 9 (P.T.A.B. July 9, 2021).....7

Samsung Elecs. Am., Inc. v. Prisua Eng'g Corp.,
948 F.3d 1342 (Fed. Cir. 2020) 7

Shure Inc. v. Clearone, Inc.,
PGR2020-00079, Paper 14 (February 16, 2021).....78

Spherix Inc. v. Matal,
703 F. App'x 982 (Fed. Cir. 2017) 7

Target Corp. v. Proxicom Wireless, LLC,
IPR2020-00904, Paper 11 (P.T.A.B. Nov. 10, 2020).....7

Vibrant Media v. Gen. Elec. Co.,
IPR2013-00172, Paper 50, 10 (P.T.A.B. July 28, 2014).....7

VMware, Inc. v. Intellectual Ventures I LLC,
IPR2020- 00470.....76

Statutes

35 U.S.C. § 102(a) 13, 14, 15

35 U.S.C. § 102(b) 8, 13, 14

35 U.S.C. § 103 3

Other Authorities

37 C.F.R. § 42.15 2

37 C.F.R. § 42.22 2

37 C.F.R. § 42.100(b) 6

37 C.F.R. § 42.104 2

37 C.F.R. § 42.104(a).....2

37 C.F.R. § 42.104(b) 2

37 C.F.R. § 42.105 2

37 C.F.R. § 42.106 2

TABLE OF ABBREVIATIONS AND CONVENTIONS

Abbreviation	Meaning
Decl.	Declaration of Dr. Vojin Oklobdzija (Ex. 1003)
Halbert	U.S Patent Application Publication No. 2002/0112119 to Halbert et al. (Ex. 1005)
JESD21-C	PC2100 and PC1600 DDR SDRAM Registered DIMM Design Specification, JEDEC Standard 21-C (January 2002) (Ex. 1006)
JESD79-2A	DDR2 SDRAM Specification, JESD79-2A (January 2004) (Ex. 1007)

PETITIONER'S EXHIBIT LIST

Ex. No.	Brief Description
1001	U.S. Patent No. 10,489,314
1002	File History of U.S. Patent No. 10,489,314
1003	Declaration of Dr. Vojin Oklobdzija
1004	Curriculum Vitae of Dr. Vojin Oklobdzija
1005	U.S Patent Application Publication No. 2002/0112119 to Halbert et al.
1006	PC2100 and PC1600 DDR SDRAM Registered DIMM Design Specification, JEDEC Standard 21-C (January 2002)
1007	DDR2 SDRAM Specification, JESD79-2A (January 2004)
1008	Netlist Proposed Claim Construction in *Netlist, Inc. v. Micron Technology, Inc. et al.*, Case No. 6:21-cv-00431 (W.D. Tex.)
1009	Micron's Proposed Claim Construction in *Netlist, Inc. v. Micron Technology, Inc. et al.*, Case No. 6:21-cv-00431 (W.D. Tex.)
1010	Defendants' Stipulation of Invalidity Contentions for U.S. Patent No. 10,489,314, *Netlist, Inc. v. Micron Technology, Inc. et al.*, Case No. 1:22-cv-00136 (W.D. Tex.)
1011	Pre-*Markman* Scheduling Order, *Netlist, Inc. v. Micron Technology, Inc. et al.*, Case No. 1:22-cv-00136 (W.D. Tex.)

CLAIM LISTING

Ref. No.	Listing of Challenged Claims
Limitation [1.1a]	A memory module operable in a computer system to communicate data with a memory controller of the computer system at a specified data rate via a N-bit wide data bus in response to memory commands received from the memory controller,
Limitation [1.1b]	the memory commands including a first memory command and a subsequent second memory command, the first memory command to cause the memory module to receive or output a first burst of N-bit wide data signals and a first burst of data strobes and the second memory command to cause the memory module to receive or output a second burst of N-bit wide data signals and a second burst of data strobes, the memory module comprising:
Limitation [1.2]	a printed circuit board having a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system;
Limitation [1.3]	a plurality of memory integrated circuits mounted on the printed circuit board and arranged in a plurality of N-bit wide ranks,
Limitation [1.4]	wherein the plurality of N-bit wide ranks include a first rank configured to receive or output the first burst of N-bit wide data signals and the first burst of data strobes at the specified data rate in response to the first memory command, and a second rank configured to receive or output the second burst of N-bit wide data signals and the second burst of data strobes at the specified data rate in response to the second memory command;
Limitation [1.4a]	wherein the plurality of N-bit wide ranks include a first rank configured to receive or output the first burst of N-bit wide data signals and the first burst of data strobes at the specified data rate in response to the first memory command,

Ref. No.	Listing of Challenged Claims
Limitation [1.4b]	and a second rank configured to receive or output the second burst of N-bit wide data signals and the second burst of data strobes at the specified data rate in response to the second memory command;
Limitation [1.5]	circuitry coupled between the plurality of N-bit wide ranks and the N-bit wide data bus; and
Limitation [1.6]	logic coupled to the circuitry and configured to respond to the first memory command by providing first control signals to the circuitry and to subsequently respond to the second memory command by providing second control signals to the circuitry,
Limitation [1.7]	wherein the circuitry is configured to enable data transfers through the circuitry in response to the first control signals and subsequently in response to the second control signals,
Limitation [1.8]	wherein respective N-bit wide data signals of the first burst of N-bit wide data signals and respective data strobes of the first burst of data strobes are transferred at the specified data rate between the first rank and the N-bit wide data bus through the circuitry,
Limitation [1.9]	and wherein respective N-bit wide data signals of the second burst of N-bit wide data signals and respective data strobes of the second burst of data strobes are transferred at the specified data rate between the second rank and the N-bit wide data bus through the circuitry;
Limitation [1.10]	wherein the data transfers through the circuitry are registered data transfers enabled in accordance with an overall CAS latency of the memory module,
Limitation [1.11]	and the circuitry is configured to add a predetermined amount of time delay for each registered data transfer through the circuitry so that the overall CAS latency of the memory module is greater than an actual operational CAS latency of each of the plurality of memory integrated circuits.

Ref. No.	Listing of Challenged Claims
Limitation [2.1]	The memory module of claim 1, wherein each of the plurality memory integrated circuits has a corresponding load,
Limitation [2.2]	and wherein the circuitry is configured to isolate the loads of the plurality of memory integrated circuits from the memory controller.
Limitation [3.1]	The memory module of claim 1, wherein the logic is coupled to the printed circuit board and is further configured to receive from the memory controller a first set of input address and control signals associated with the first memory command and to respond to the first memory command by outputting a first set of registered address and control signals,
Limitation [3.2]	and wherein the logic is further configured to subsequently receive from the memory controller a second set of input address and control signals associated with the second memory command and to respond to the second memory command by outputting a second set of registered address and control signals,
Limitation [3.3]	the first set of input address and control signals including a first set of input chip select signals corresponding to respective ranks of the plurality of ranks
Limitation [3.4]	and the second set of input address and control signals including a second set of input chip select signals corresponding to respective ranks of the plurality of ranks,
Limitation [3.5]	the first set of registered address and control signals including a first plurality of registered chip select signals corresponding to respective ones of the first plurality of input chip select signals,
Limitation [3.6]	the second set of registered address and control signals including a second plurality of registered chip select signals corresponding to respective ones of the second plurality of input chip select signals,

Ref. No.	Listing of Challenged Claims
Limitation [3.7]	the first set of registered chip select signals including a first registered chip select signal having an active signal value and one or more other registered chip select signals each having a non-active signal value,
Limitation [3.8]	The second set of registered chip select signals including a second registered chip select signal having an active signal value and one or more other registered chip select signals each having a non-active signal value,
Limitation [3.9]	and wherein the logic is configured to output the first registered chip select signal to the first rank and to output the second registered chip select signal to the second rank.
Limitation [5.1]	The memory module of claim 1, wherein the memory module is configured to receive from the memory controller an on-die-termination (ODT) signal,
Limitation [5.2]	wherein each of the plurality of memory integrated circuits includes an ODT circuit,
Limitation [5.3]	the memory module further comprising a termination circuit external to any of the plurality of memory integrated circuits,
Limitation [5.4]	wherein the termination circuit is configured to receive the ODT signal and is coupled to the ODT circuit of at least one of the plurality of memory integrated circuits,
Limitation [5.5]	wherein the termination circuit is configured to provide external termination for the at least one of the plurality of memory integrated circuits in response to the ODT signal,
Limitation [5.6]	and wherein the ODT circuit of the at least one of the plurality of memory integrated circuits is disabled.
Claim 6	The memory module of claim 1, wherein the circuitry includes logic pipelines configured to enable the data transfers through the circuitry in response to the first control

Ref. No.	Listing of Challenged Claims
	signals and subsequently in response to the second control signals.
Claim 8	The memory module of claim 1, wherein N is 64 or 72.
Limitation [9.1]	The memory module of claim 1, wherein each rank of the plurality of ranks is 72-bits wide,
Limitation [9.2]	wherein each rank of the plurality of N-bit wide ranks includes 18 4-bit wide memory integrated circuits configured in 9 pairs,
Limitation [9.3]	wherein a first pair of memory integrated circuits in the first rank is configured to communicate a respective byte of the first burst of N-bit wide data signals in each time interval of a first plurality of time intervals,
Limitation [9.4]	and wherein a second pair of memory integrated circuits in the second rank is configured to communicate a respective byte of the second burst of N-bit wide data signals in each time interval of a second plurality of time intervals.
Limitation [10.1]	The memory module of claim 9, wherein the first pair of memory integrated circuits are configured to simulate an 8-bit wide memory device,
Limitation [10.2]	and the second pair of memory integrated circuits are configured to simulate another 8-bit wide memory device.
Limitation [12.1]	The memory module of claim 1, wherein the respective N-bit wide data signals of the first burst of N-bit wide data signals and the respective data strobes of the first burst of data strobes are transferred through the circuitry during respective time intervals of a first plurality of time intervals,
Limitation [12.2]	and wherein the respective N-bit wide data signals of the second burst of N-bit wide data signals and the respective data strobes of the second burst of data strobes are transferred through the circuitry during respective time intervals of a second plurality of time intervals.

Ref. No.	Listing of Challenged Claims
Limitation [13.1]	The memory module of claim 1, further comprising a phase locked loop clock driver configured to output a clock signal in response to one or more signals received from the memory controller,
Limitation [13.2]	wherein the predetermined amount of time delay is at least one clock cycle time delay.
Limitation [14.1]	The memory module of claim 13, wherein the memory integrated circuits are dynamic random access memory integrated circuits configured to operate synchronously with the clock signal,
Limitation [14.2]	wherein each memory integrated circuit in the first rank is configured receive [*sic*] or output a respective set of bits of the first burst of N-bit wide data signals on both edges of each of a respective set of data strobes of the first burst of data strobes,
Limitation [14.3]	and wherein each memory integrated circuit in the second rank is configured receive [*sic*] or output a respective set of bits of the second burst of N-bit wide data signals on both edges of each of a respective set of data strobes of the second burst of data strobes.

I. Introduction

Petitioners Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC ("Petitioners"/"Micron") request *inter partes* review ("IPR") of claims 1-3, 5-6, 8-10, and 12-14 ("Challenged Claims") of U.S. Patent No. 10,489,314 ("'314 patent").

The '314 patent is generally directed to a memory module[1] that is connectable to a computer's memory controller. The memory module includes ranks of memory devices[2] and register buffers that separate the memory devices from the connections to the memory controller. The patent observes that the addition of register buffers will add a clock cycle time delay that results in a memory module with an overall Column Address Strobe ("CAS") latency ("CL") greater than the actual operational CL of the memory devices.

The fatal flaw to the Challenged Claims is that memory modules as claimed were well-known. For example, U.S. Patent Application Publication No. 2002/0112119 to Halbert et al. ("Halbert") discloses a very similar memory module with ranks of memory devices separated from a memory controller by register

[1] For example, a dual in-line memory module ("DIMM") card.

[2] For example, dynamic random access memory ("DRAM") cells.

buffers. Indeed, the Board in IPR2017-00549 relied upon Halbert to find challenged claims in the '314 patent's extended family unpatentable.

As explained in this Petition, the Challenged Claims would not have been allowed if Halbert had been substantively evaluated by the Examiner during prosecution. The Challenged Claims are unpatentable and should be cancelled.

II. Requirements for *Inter Partes* Review

This Petition complies with all statutory requirements, as well as 37 C.F.R. §§ 42.104, 42.105, and 42.15, and should be accorded a filing date pursuant to 37 C.F.R. § 42.106. The required fee is being paid electronically through PTAB E2E.

A. The '314 Patent Is Available For *Inter Partes* Review

As required by 37 C.F.R. § 42.104(a), Petitioners certify that the '314 patent "is available for [IPR] and that the Petitioners are not barred or estopped from requesting an [IPR] challenging the patent claims on the grounds identified in the petition." Petitioners certify that this Petition is filed within one year of the date of service of Netlist's complaint—June 15, 2021—alleging infringement of the '314 patent. No Petitioner, or party in privity with Petitioners, has filed a civil action challenging the validity of any claim of this patent.

B. Grounds

Under 37 C.F.R. §§ 42.104(b) and 42.22, Petitioners request that the Board institute this IPR on the Challenged Claims of the '314 patent and cancel those

claims as unpatentable for obviousness under pre-AIA 35 U.S.C. § 103 on the following grounds:

Ground	Claim	Basis for Unpatentability
1	1-2, 6, 8, and 12-14	Halbert in view of a POSITA's knowledge
2	3 and 9-10	Halbert in view of JEDEC Standard 21-C
3	5	Halbert in view of JEDEC Standard JESD79-2A

III. The '314 Patent

A. Earliest Effective Filing Date

The '314 patent claims priority through a series of applications, the earliest being provisional application No. 60/550,668, filed on March 5, 2004. For purposes of this Petition, Petitioners assume an effective filing date of March 5, 2004.

B. Level of Ordinary Skill in the Art

As of March 2004, a person of ordinary skill in the art ("POSITA") would have been someone with an advanced degree in electrical or computer engineering and at least two years working in the field, or a bachelor's degree in such engineering disciplines and at least three years working the field. Decl., ¶ 52. Such a person would have been knowledgeable about the design and operation of computer memories, most particularly DRAM and SDRAM devices that were compliant with various standards of the day, and how they interact with other components of a computer system, such as memory controllers. *Id.* He or she would also have been

familiar with the structure and operation of circuitry used to access and control computer memories, including sophisticated circuits such as ASICs and CPLDs and less sophisticated circuits such as tri-state buffers, flip flops, and registers. *Id.* The references cited in this Petition and the experience of Dr. Vojin Oklobdzija, as described in his expert declaration, reflect this level of skill in the art.

C. Overview of the '314 Patent

The '314 patent relates to memory modules that are described in terms of single in-line memory modules ("SIMMs"), DIMMs, and other types of memory cards of various sizes. Ex. 1001, 6:14-23, 6:31-38. The memory modules are described as a "printed circuit board" containing "edge connectors" for coupling to a "module slot of a computer system." *Id.*, 6:25-28. The memory modules communicate with a host computer's "memory controller" through this module slot and via a "data bus." *Id.*, 3:17-20.

The memory modules include "memory devices," such as random access memory, DRAM, and other types of commercially available devices. *Id.*, 6:39-58. The modules are arranged in ranks, e.g., Fig. 9B depicts two ranks (32a-32b) and Fig. 9A depicts four ranks (32a-32d):

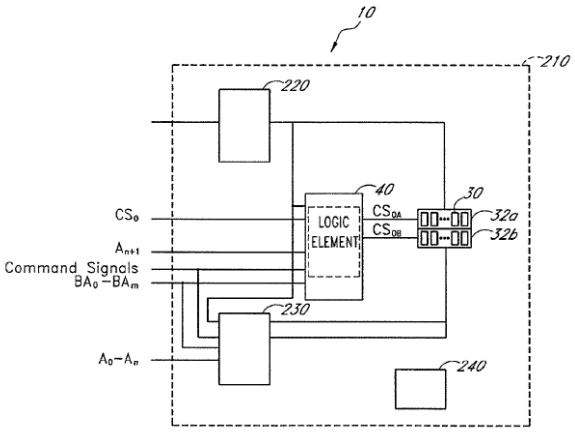


FIG. 9B

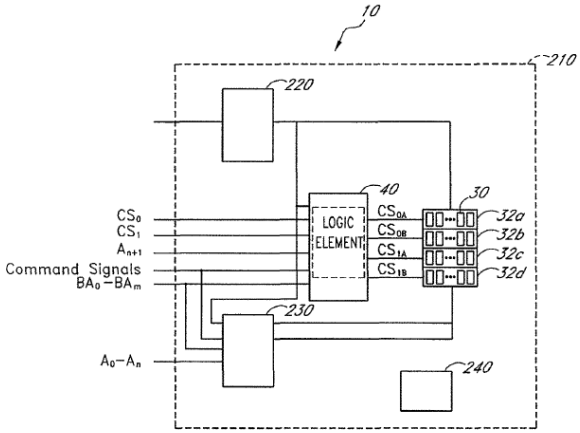


FIG. 9A

Id., Figs. 9A-9B.

As depicted in Figs. 9A-9B, the memory devices are coupled to "circuit" 40 and "register" 230. Circuit 40 "receives a set of input address and command signals" and "generates a set of output address and command signals in response." *Id.*, 16:27-32. Register 230 "receives and buffers a plurality of command signals and address signals." *Id.*, 16:45-46. Also depicted is "SPD" 240 which communicates data regarding various attributes of the memory module to the "basic input/output (BIOS) of the computer system so that the computer system is informed of the memory capacity." *Id.*, 19:36-47.

The '314 patent describes an embodiment where the SPD "reports a CL which has one more cycle than does the actual operational CL of the memory devices." *Id.*, 22:41-43. This SPD reporting feature is described in terms of the one clock cycle delay caused by transferring data through a register buffer included between the

module's memory devices and its connections to the host memory controller. *Id.*, 22:43-62.

D. Relevant Prosecution History of the '314 Patent Family

No office action rejections were issued during prosecution of the '314 patent. Halbert and JEDEC Standard 21-C ("JESD21-C") relied upon herein were identified on an IDS by Netlist during prosecution. Neither were substantively addressed, or even discussed, by the Examiner. Both references, however, were substantively evaluated by the Board in IPRs that found claims in the '314 patent's family unpatentable.[3]

IV. Claim Construction

The Board construes claims under the same standard used in civil actions in federal district court. 37 C.F.R. § 42.100(b). The district court for the related litigations has not yet construed the claim terms. The parties' proposed constructions from those actions are set forth in Exs. 1008-1009.

[3] The Board examined Halbert in IPR2017-00549 and JESD21-C in IPR2014-00883, IPR2015-01021, and IPR2015-01020. The challenged patents in these proceedings (U.S. Patent Nos. 8,756,364, 8,081,536, and 7,881,150) and the '314 patent challenged herein all claim priority to provisional Application Nos. 60/550,668, 60/575,595, and 60/590,038; and U.S. Patent Nos. 7,289,386 and 7,286,436.

The parties' construction disputes from the related litigations do not affect the outcome of this Petition with respect to any claim.

First, for the terms "overall CAS latency …" and "actual operational CAS latency …," the prior art invalidates the claims under either side's proposed constructions, as shown herein. Petitioners' analysis identifies how the claims are invalid under both sides' proposed constructions for these terms. Second, with respect to the terms that Petitioners contend are indefinite in the related litigations, Petitioners use Netlist's "plain meaning" interpretations herein. To be clear, Petitioners are not asking the Board to find any claim indefinite for the purposes of this Petition. The Board and Federal Circuit have approved of this procedure in several matters. *See, e.g., Micron Tech., Inc. et al. v. Unification Techs. LLC*, IPR2021-00344, Paper 9 at 10-11 (P.T.A.B. July 9, 2021); *Spherix Inc. v. Matal*, 703 F. App'x 982, 983 (Fed. Cir. 2017) (approving petitioner's proposal of patent owner's claim interpretations); *Target Corp. v. Proxicom Wireless, LLC*, IPR2020-00904, Paper 11 at 12 (P.T.A.B. Nov. 10, 2020) ("Petitioner's alternative pleading before a district court is common practice, especially where it concerns issues outside the scope of [IPR]."); *Samsung Elecs. Am., Inc. v. Prisua Eng'g Corp*., 948 F.3d 1342, 1355 (Fed. Cir. 2020); *Vibrant Media v. Gen. Elec. Co*., No. IPR2013-00172, Paper 50, 10 (P.T.A.B. July 28, 2014).

V. Grounds for Unpatentability

The Challenged Claims are unpatentable based on three different grounds. Ground 1 establishes that claims 1-2, 6, 8, and 12-14 are obvious over Halbert in view of a POSITA's knowledge. Ground 2 establishes that claims 3 and 9-10 are obvious over Halbert in view of JESD21-C. Ground 3 establishes that claim 5 is obvious over Halbert in view of JEDEC Standard JESD79-2A ("JESD79-2A"). These references and Grounds are further discussed below.

A. Overview of the Prior Art

1. Halbert

Halbert is entitled "Dual-Port Buffer-to-Memory Interface." Halbert was filed on March 13, 2002, published on August 15, 2002, and qualifies as prior art under at least pre-AIA 35 U.S.C. § 102(b).

Halbert discloses "a new memory module architecture" for a typical memory system configuration, e.g., shown in Fig. 1 below. Halbert, Abstract, [0004].

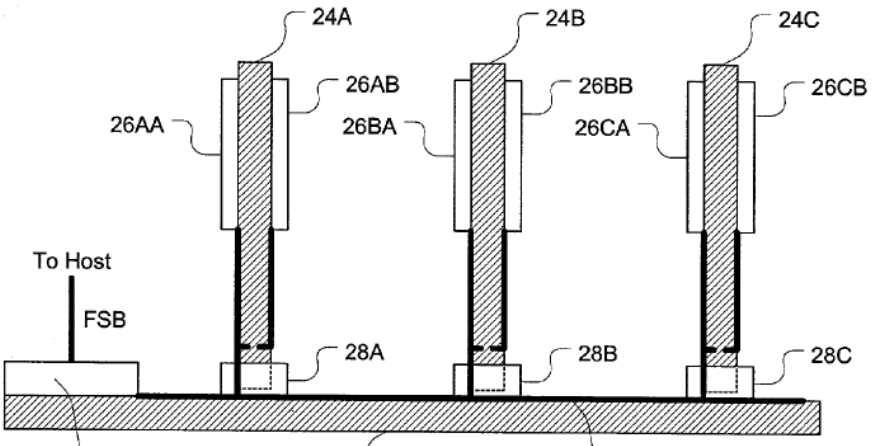


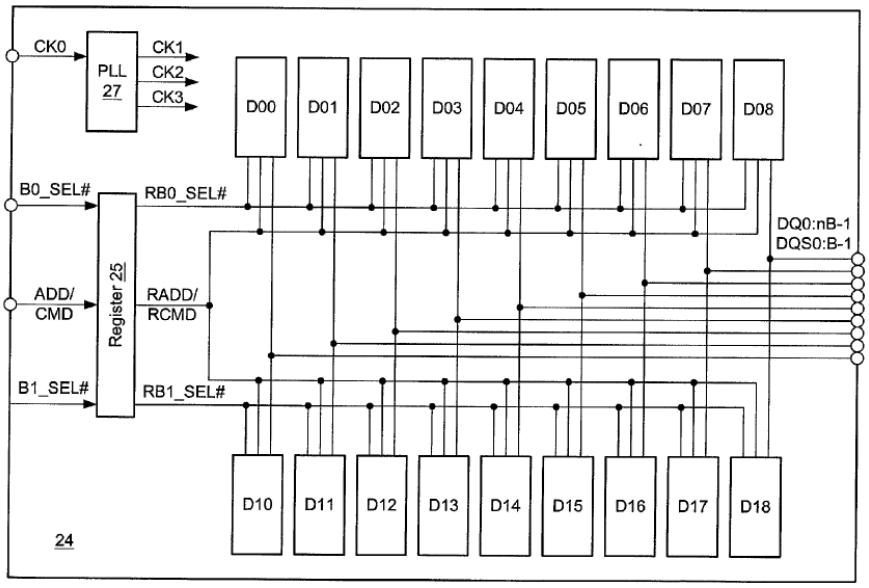
Fig. 1 (Prior Art)

Halbert, Fig. 1.

Halbert's Fig. 1 illustrates an exemplary system with three memory modules 24A-C inserted into corresponding sockets 28A-C and connected to a memory bus 22, which connects to a system memory controller 20. Halbert, [0006]-[0007]. The memory bus 22 carries memory signals, which include "clock and control signals, address signals, command signals, and data signals." *Id*., [0005]; Decl., ¶ 69.

Halbert illustrates an exemplary prior art module, such as "a registered DIMM 24 containing eighteen memory devices arranged in two banks, one containing devices D00-D08 and the other containing devices D10-D18," as shown in Fig. 2 below. Halbert, [0009]; Decl., ¶ 70.

Fig. 2
(Prior Art)

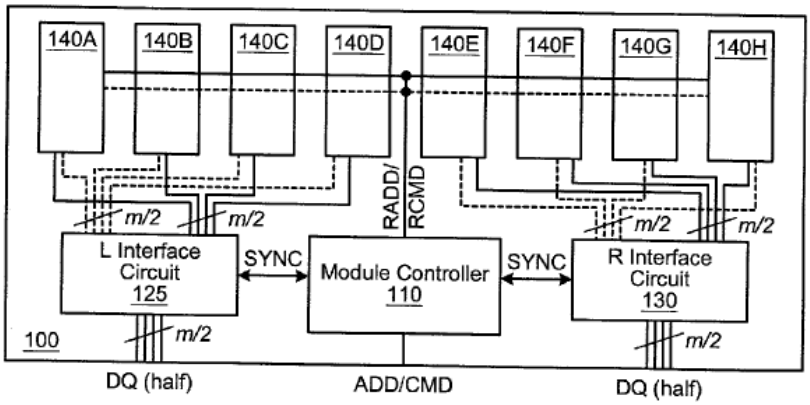


Halbert, Fig. 2.

The prior art DIMM 24 has a register 25 that latches on the address and command signals ADD/CMD and re-drives those signals onto the module's address/command bus connected to the memory devices D00-D18. Halbert, Fig. 2. The register 25 receives bank select signals B0_SEL# and B1_SEL# and provides registered versions of those signals to chip select pins of corresponding banks of memory devices. *Id*. The data lines from each bank of memory devices are connected to a common set of DQ lines carrying data and DQS lines carrying data strobes. *Id*. Each device has a data width of n (4, 8, or 16) bits that add up to the total of n*B data lines, where B is the number of memory devices per bank (nine in Fig. 2). This prior art module has data lines directly connecting the memory chips to memory bus 22. *Id*.; Decl., ¶ 71.

Halbert discloses a new module architecture that can be implemented to be "transparent to the memory system and to the memory devices … [which] allows for an embodiment that is compatible with an existing memory controller/bus and with existing memory devices." Halbert, [0023]. An exemplary implementation of Halbert's inventive module is shown in Figs. 7-8 below. Decl., ¶ 72.

Fig. 7



Halbert, Fig. 7.

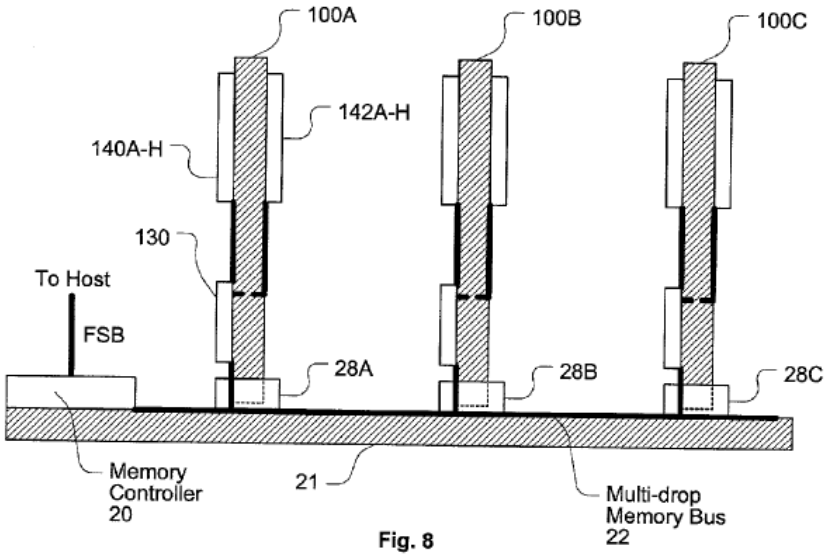


Fig. 8

Id., Fig. 8.

As depicted in Figs. 7-8, the memory module 100 has a module controller 110 which, like the register 25 in the prior art module, receives the address and command signals from the memory controller and provides registered versions of those signals to two ranks of memory devices 140A-H and 142A-H. Halbert, [0048]-[0049]. Memory module 100, as illustrated by modules 100A-C in Fig. 8, can be attached to

memory bus sockets 28A-C. Unlike the prior art module, however, memory module 100 includes interface circuits (shown as interface circuits 125 and 130 in Fig. 7 and data interface circuit 120 in Fig. 4) between memory bus 22, on one side, and corresponding memory devices in ranks 140 and 142, on the other side. The interface circuits are controlled by the module controller 110 through control signals. Halbert, [0048]; Decl., ¶ 73.

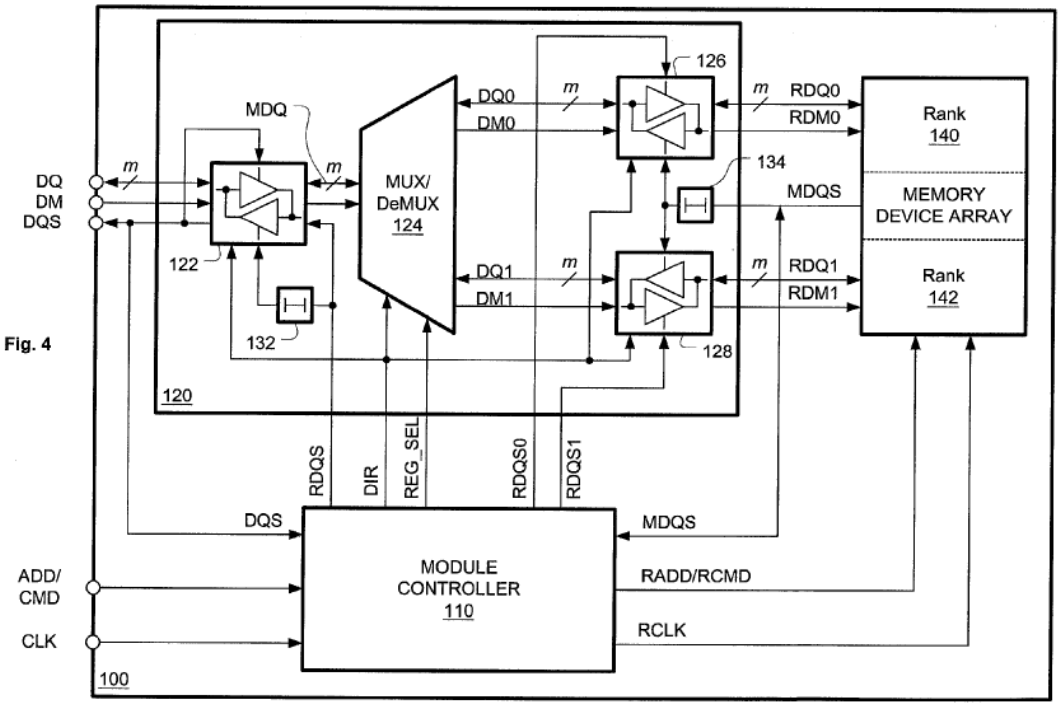


Fig. 4

Halbert, Fig. 4.

Referring to Fig. 4, on the memory bus side (to the left in Fig. 4), the interface circuit 120 has a bi-directional buffer 122 that receives and drives data signals DQ from/to the system memory controller. Halbert, [0031]. The bi-directional buffer 122 can also drive data strobe signals DQS onto the memory bus. *Id*. On the

memory rank side (to the right in Fig. 4), the interface circuit 120 has two bi-directional registers 126 and 128 to connect to the memory ranks 140 and 142, respectively. *Id*., [0032]. Signals communicated between buffer 122 and registers 126 and 128 are switched by a multiplexer/demultiplexer 124. Decl., ¶ 74.

The interface circuit 120 is controlled by the module controller 110 using signals. Halbert, [0034]-[0036]. "For instance, direction signal DIR specifies whether data flow is towards the memory array (TO) or away from the memory array (AWAY)." *Id*., [0034]. "The register select signal REG_SEL, in the AWAY mode, determines whether DQ0 [from Rank 140] or DQ1 [from Rank 142] will be supplied to buffer 122 … [which] drives that data onto the memory data bus." *Id*., [0035]. "In the TO mode, REG_SEL determines which of registers 126 and 128 will receive DQ at each memory bus clock cycle." *Id*., [0036]; Decl., ¶ 75.

2. Overview of JESD21-C

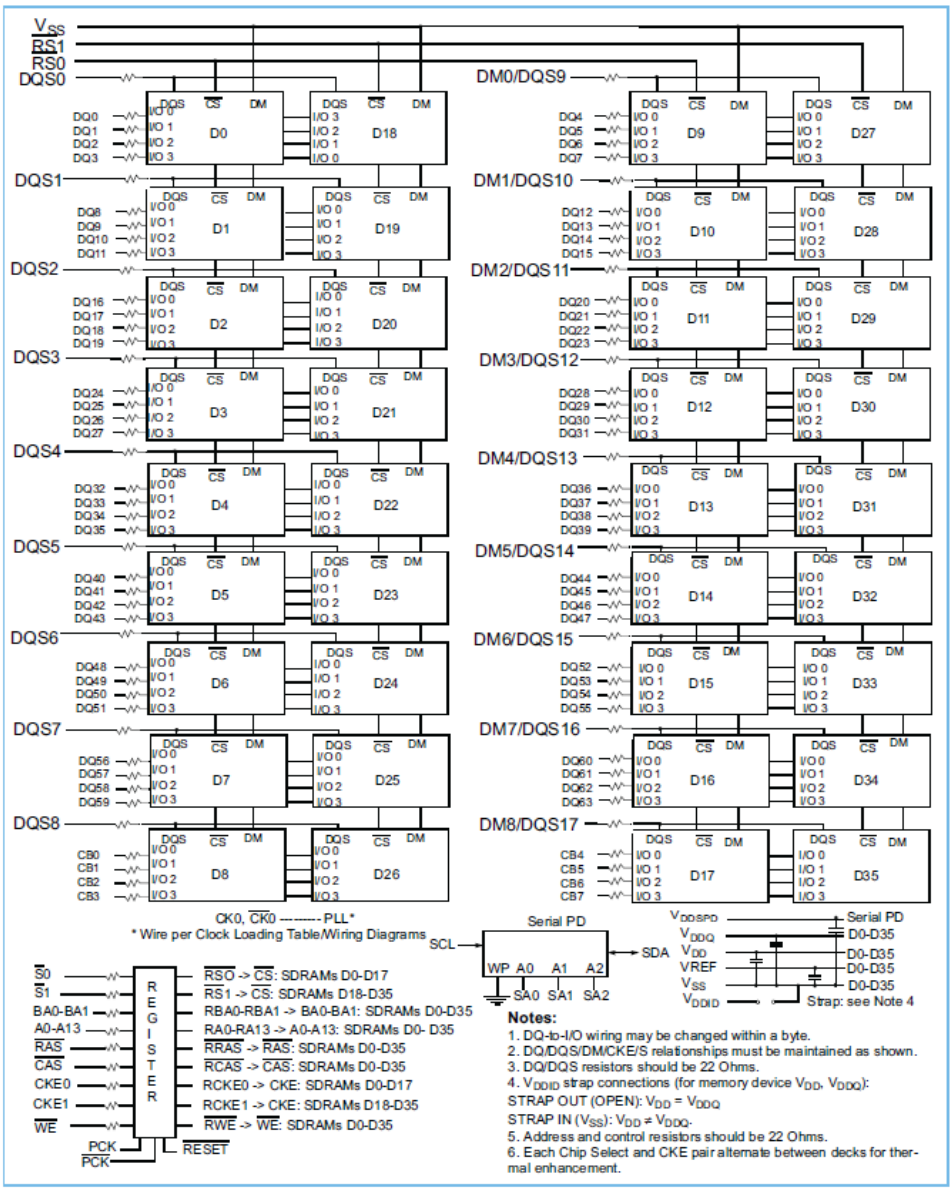
JESD21-C is an SDRAM Registered DIMM Design Specification. JESD21-C published in January 2002 and qualifies as prior art under pre-AIA 35 U.S.C. §§ 102(a)-(b).

JESD21-C is a specification that "defines the electrical and mechanical requirements for specific types of SDRAM DIMMs that are intended for use as main memory when installed in systems such as servers and workstations." JESD21-C,

5. JESD21-C provides reference design examples to "provide an initial basis for Registered DIMM designs." *Id.*; Decl., ¶ 79

JESD21-C provides several example architecture block diagrams of DDR SDRAMs. An example architecture block diagram of two physical banks of x4 DDR SDRAMs is shown below.

Block Diagram: Raw Card Version N (Populated as two physical banks of x4 DDR SDRAMs)

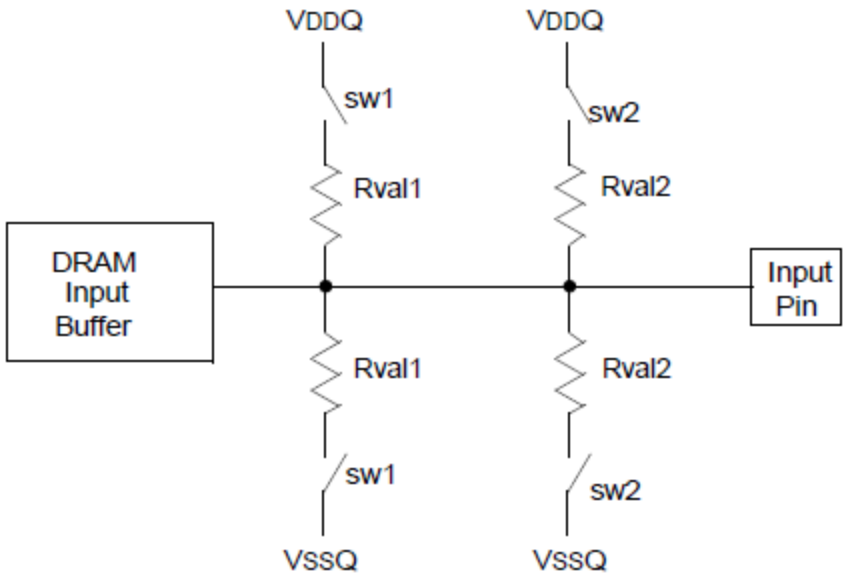


JESD21-C, 15. Raw Card Version N shows eighteen 4-bit wide memory devices configured in nine pairs. The D0-D8 and D9-D17 memory devices are selected for data transfers by RS0[bar], and the D18-D26 and D27-D35 memory devices are selected for data transfers by RS1[bar]. Decl., ¶ 81.

3. Overview of JESD79-2A

JESD79-2A is a DDR2 SDRAM Specification published by the JEDEC Solid State Technology Association in January 2004 and qualifies as prior art under pre-AIA 35 U.S.C. § 102(a).

JESD79-2A helps facilitate interchangeability and improvement of DDR2 SDRAM products. JESD79-2A, 2. It provides "a sound approach to product specification and application, principally from the solid state device manufacturer viewpoint." *Id*. JESD79-2A provides a functional description of the input/output pins to DDR2 SDRAMs. *See* JESD79-2A, 14. One of the inputs disclosed is the on-die termination ("ODT") pin. A functional representation of the ODT circuit with ODT input pin is shown in Fig. 15 below.



Switch sw1 or sw2 is enabled by ODT pin.
Selection between sw1 or sw2 is determined by "Rtt (nominal)" in EMRS
Termination included on all DQs, DM, DQS, $\overline{\text{DQS}}$, RDQS, and $\overline{\text{RDQS}}$ pins.
Target Rtt (ohm) = (Rval1) / 2 or (Rval2) / 2

Figure 15 — Functional Representation of ODT

JESD79-2A, Fig. 15; Decl., ¶¶ 83, 86.

JESD79-2A describes ODT as "a feature that allows a DRAM to turn on/off termination resistance for each DQ, DQS/DQS, RDQS/RDQS, and DM signal for x4x8 configurations via the ODT control pin." JESD79-2A, 26. The ODT is a beneficial feature for improving "signal integrity of the memory channel by allowing the DRAM controller to independently turn on/off termination resistance for any or all DRAM devices." *Id.*; Decl., ¶ 87.

B. Ground 1: Halbert in View of a POSITA's knowledge Render Claims 1-2, 6, 8, and 12-14 Obvious

1. Claim 1

a. Limitation [1.1]

Halbert discloses Limitation [1.1a]. Halbert's Fig. 8 depicts "three of the [memory] modules depicted in FIG. 7 arranged in a memory system with a primary memory controller 20 and a multi-drop memory bus 22." Halbert, [0049].

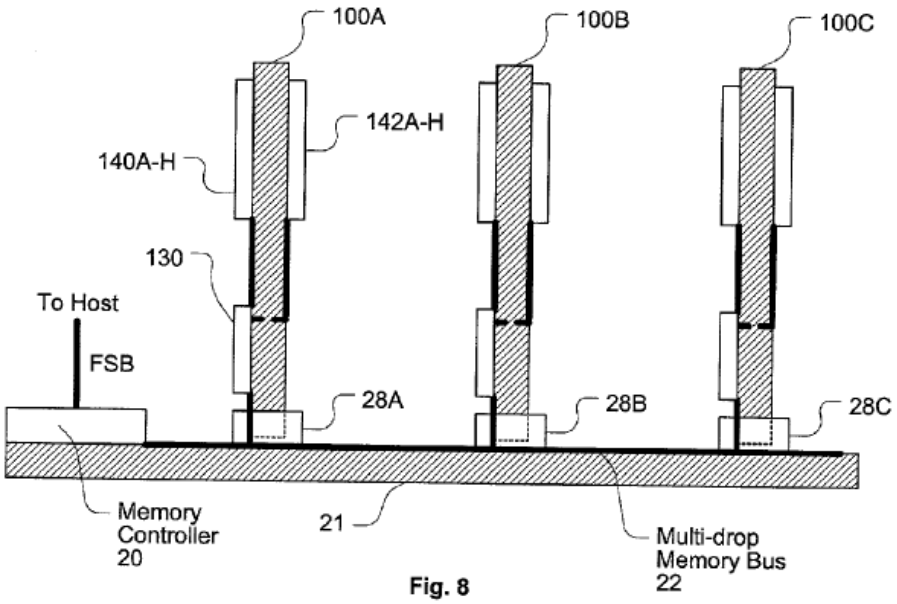


Fig. 8

Id., Fig. 8; Decl., ¶ 92.

Halbert further discloses the components of a memory module, e.g., as depicted in Fig. 4 below.

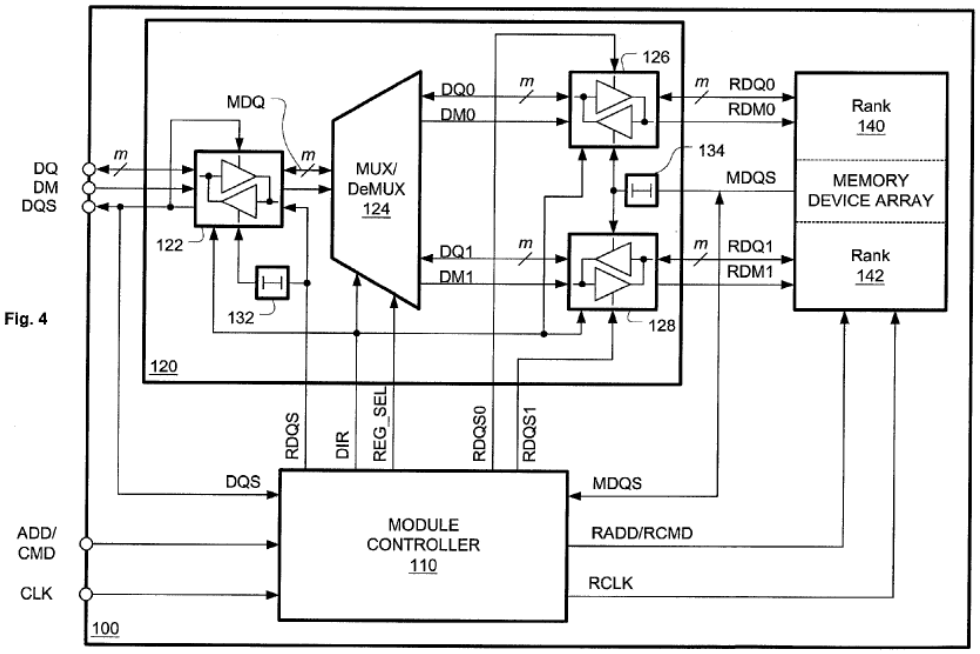


Fig. 4

Halbert, Fig. 4. Memory module 100 has a data interface circuit 120 that "provides for m-bit-wide data transfers between the module and the system memory data bus, and for R×m-bit-wide data transfers between the interface circuit and the memory device array. In FIG. 4, R=2, i.e., the memory device array comprises two memory device ranks 140 and 142." Halbert, [0030]. Data transfers are in response to memory commands received from memory controller 20. "Command signals instruct a memory device as to what type of operation is to be performed, e.g., read, write, refresh." Halbert, [0005]; Decl., ¶¶ 93-94.

Halbert discloses that "one embodiment describes a DIMM that can, with the same type of devices, number of devices, and data signal pins as the dual-bank registered DIMM, provide twice the data rate of the registered DIMM." Halbert, [0024]. A POSITA would have understood that Halbert's memory module 100

enables data transfers at the specified data rate between the system memory data bus and the memory module 100, i.e., at twice the data rate of the registered DIMM. Decl., ¶ 95.

Halbert discloses Limitation [1.1b]. Halbert's memory module 100 receives and outputs bursts of N-bit wide data signals and data strobes. In FIG. 4, "[a]n m-bit-wide path through buffer 122 receives and drives data signals DQ on the system memory data bus. … Finally, a data strobe signal DQS can be driven by buffer 122 onto the memory data bus." Halbert, [0031]; *see also id*., [0032]; Decl., ¶ 96.

Memory module 100's outputting and receiving of first and second bursts of N-bit wide data signals and data strobes is caused by *a first/second memory command, i.e., a read command*, and subsequent *write command*. Halbert discloses that "[i]n the ACTIVE state, controller 110 scans the command bus for READ or WRITE commands." Halbert, [0037]. A read command causes memory module 100 to output data signals and strobes. "In FIG. 4, either data signals DQ0 (from register 126) or data signals DQ1 (from register 128) can be multiplexed to buffer 122 when the module is reading from memory device array 140/142." *Id*., [0033]. In the AWAY (read) mode, "register data strobe RDQS is functional. When RDQS transitions, buffer 122 latches data from MUX 124 and drives that data onto the memory data bus." *Id*., [0035], Fig. 5. RDQS is latched into buffer 122 and appears at the memory bus port as DQS. *Id*., [0041]. Memory device array 140/142 also

outputs memory data strobe MDQS as part of the read operation. "MDQS will comprise multiple strobes, each device in device array 140/142 supplying at least one strobe synchronized to its data signals." *Id*., [0038]; Decl., ¶ 97. The receipt and output of data strobes MDQS by each of the memory devices meets Netlist's proposed alternative construction of "burst of data strobes" because the data strobe signals MDQS have "successive rising and falling edges, each edge being associated with a data bit." Decl., ¶ 97 (Figs. 5 and 6 depict data bits associated with the rising and falling edges of MDQS).

Halbert discloses that a write command ("*second memory command*") causes memory module 100 to receive data signals and data strobes. "[W]hen the module is writing to the memory device array, data signals MDQ from buffer 122 can be channeled to either DQ0 or DQ1." Halbert, [0033]. In the TO (write) mode, "[c]ontroller 110 strobes the memory device array, using the memory data strobe MDQS, to signal the array to write data from buses RDQ0 and RDQ1." *Id*., [0036], Fig. 6; Decl., ¶ 98.

Alternatively, memory module 100's outputting of first and second bursts of N-bit wide data signals and strobes can be caused by *a first/second memory command, i.e., a read command* and a *subsequent read command*. Read commands cause memory module 100 to output data signals and data strobes from memory device array 140 on DQ0 (from register 126) during a first bus clock cycle and from

memory device array 142 on DQ1 (from register 128) during the following bus clock cycle. *Id*., [0035] ("For instance, REG_SEL can first select, e.g., DQ0 during a first bus clock cycle, and then DQ1 during the following bus clock cycle."); Decl., ¶ 99. Memory device array 140/142 also outputs memory data strobe MDQS as part of both read operations. "MDQS will comprise multiple strobes, each device in device array 140/142 supplying at least one strobe synchronized to its data signals." *Id*., [0038]; Decl., ¶ 100.

b. Limitation [1.2]

Halbert discloses Limitation [1.2]. *See, e.g.,* Halbert, claim 11 ("a dual-inline memory module comprising a printed circuit board capable of connection to the memory data bus via insertion of the circuit board into a card edge connector connected to the memory data bus"). Further, Halbert's Fig. 8 depicts DIMM memory modules plugged into computer sockets 28A-C. "Memory controller 20 mounts to motherboard 21 and connects to one end of the leads comprising memory bus 22. Each drop of memory bus 22 connects to an electrical terminator, or socket." *Id*., [0006].

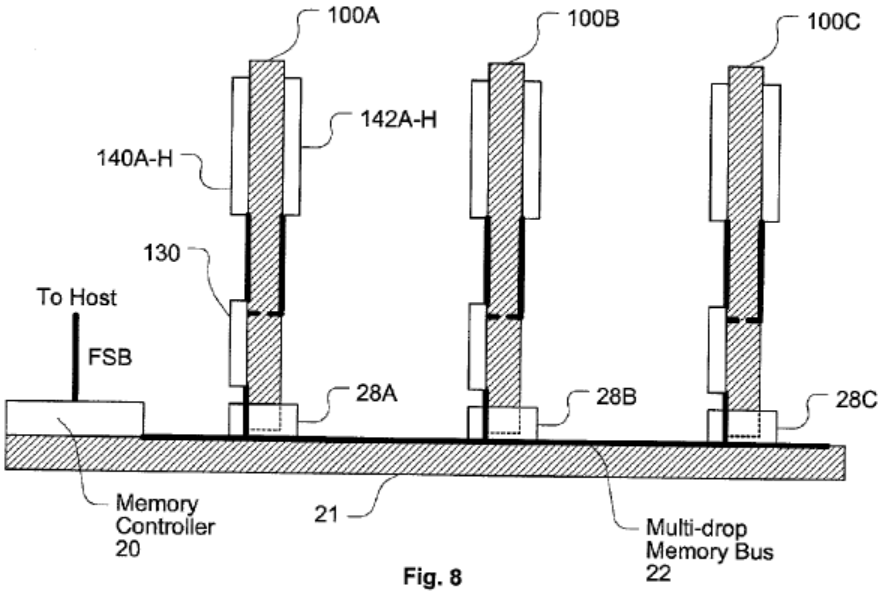


Fig. 8

Id., Fig. 8; *see also id*., [0007]; Decl., ¶¶ 102-104.

c. Limitation [1.3]

Halbert discloses Limitation [1.3]. Halbert's "FIG. 4 illustrates a block diagram for one embodiment of a memory module 100 [that includes] a memory device array 140/142." Halbert, [0027]-[0028]. Memory device array 140/142 are memory integrated circuits mounted on the printed circuit board, i.e., memory module 100, and arranged in a plurality of N-bit wide ranks. *See id*., [0030] ("In FIG. 4, R=2, i.e., the memory device array comprises two memory device ranks 140 and 142, each capable of performing m-bit-wide data transfers."); Decl., ¶ 106.

d. Limitation [1.4]

Halbert discloses Limitation [1.4a]. Halbert's memory device rank 140 can be a first rank configured to output the first burst of N-bit wide data signals and strobes at the specified rate in response to *the first memory command, i.e., the read*

command. "In FIG. 4, either data signals DQ0 (from register 126) or data signals DQ1 (from register 128) can be multiplexed to buffer 122 when the module is reading from memory device array 140/142." Halbert, [0033]. DQ0 is output from memory device array 140 on bus RDQ0. *Id*., [0038] ("Controller 110 asserts DIR (where asserted equals AWAY) sometime after passing the first READ command to device array 140/142. This assertion time can vary, but preferably occurs prior to when device array 140/142 is expected to begin driving buses RDQ0 and RDQ1."); Decl., ¶ 107.

Memory device array 140 outputs a first burst of N-bit wide data signals in response to the first memory (read) command. "In the ACTIVE state, controller 110 scans the command bus for READ or WRITE commands … At T4, a READ command (to COL a) is clocked in, causing the controller to enter a READ state." Halbert, [0037]. Data signal DQ0 is output to the memory data bus at the specified data rate. "The register select signal REG_SEL, in the AWAY mode, determines whether DQ 0 or DQ1 will be supplied to buffer 122. Data is serialized from the data registers onto the memory data bus by reading 2m bits into the data registers during one memory device read cycle, and then driving these bits, m at a time, through MUX 124." *Id*., [0035], Fig. 5. Memory device array 140 outputs the first burst of data strobes at the specified data rate, i.e., memory data strobe MDQS, as part of the read operation. "MDQS will comprise multiple strobes, each device in

device array 140/142 supplying at least one strobe synchronized to its data signals." *Id*., [0038]; Decl., ¶ 108.

Halbert discloses Limitation [1.4b]. Halbert's memory device rank 142 can be a second rank configured to receive the second burst of N-bit wide data signals and strobes at the specified rate in response to the *second memory command, i.e., the write command*. "[W]hen the module is writing to the memory device array, data signals MDQ from buffer 122 can be channeled to either DQ0 or DQ1," which is received by memory device rank 140 or 142, respectively. Halbert, [0033]. DQ1 is received at memory device array 142 on bus RDQ1. *Id*., [0036] ("Controller 110 strobes the memory device array, using the memory data strobe MDQS, to signal the array to write data from buses RDQ0 and RDQ1."); Decl., ¶ 109.

Memory device array 142 receives the second burst of N-bit wide data signals in response to the second memory (write) command. "Upon sensing the first WRITE command, module controller 110 transitions to a WRITE state." Halbert, [0043]. Data signal DQ1 is received by memory device array 142 at the specified data rate. "In the TO mode, register data strobes RDQS0 and RDQS1 are also functional. … In the following bus clock cycle, m bits are directed to register 128 by strobing RDQS1. Both register contents are then written to memory device array 140/142 during a single device write cycle." *Id*., [0036], Fig. 6. Memory device array 142 receives the second burst of data strobes at the specified data rate, i.e., memory data

strobe MDQS, as part of the write operation. "Controller 110 strobes the memory device array, using the memory data strobe MDQS, to signal the array to write data from buses RDQ0 and RDQ1." *Id*., [0036]; Decl., ¶ 110.

Alternatively, memory device rank 142 can be a second rank configured to output the second burst of N-bit wide data signals and the second burst of data strobes at the specified rate in response to *the second memory command, i.e., the second read command*. As discussed above, DQ0 is output from memory device array 140 on bus RDQ0 during a first bus clock cycle in response to a read command, and DQ1 is output from memory device array 142 on bus RDQ1 during the following bus clock cycle in response to a second read command. "For instance, REG_SEL can first select, e.g., DQ0 during a first bus clock cycle, and then DQ1 during the following bus clock cycle." Halbert, [0035]; Decl., ¶ 111.

Reading from memory device array 142 causes memory device array 142 to output the second burst of N-bit wide data signals, which occurs in response to the second memory (second read) command. Data signal DQ1 is output to the memory data bus at the specified data rate when the second read command causes REG_SEL to determine DQ1 will be supplied to buffer 122. "The register select signal REG_SEL, in the AWAY mode, determines whether DQ 0 or DQ1 will be supplied to buffer 122. … For instance, REG_SEL can first select, e.g., DQ0 during a first bus clock cycle, and then DQ1 during the following bus clock cycle." *Id*., [0035].

Memory device array 142 also outputs the second burst of data strobes at the specified data rate, i.e., memory data strobe MDQS, as part of the second read operation. "MDQS will comprise multiple strobes, each device in device array 140/142 supplying at least one strobe synchronized to its data signals." *Id.*, [0038]; Decl., ¶ 113.

e. Limitation [1.5]

Halbert discloses Limitation [1.5]. Halbert's Fig. 4 discloses the circuitry, data interface circuit 120, between the plurality of m-bit wide memory device ranks 140/142 and the m-bit wide memory data bus, shown on the left side with m-bit wide DQ connecting the memory data bus.

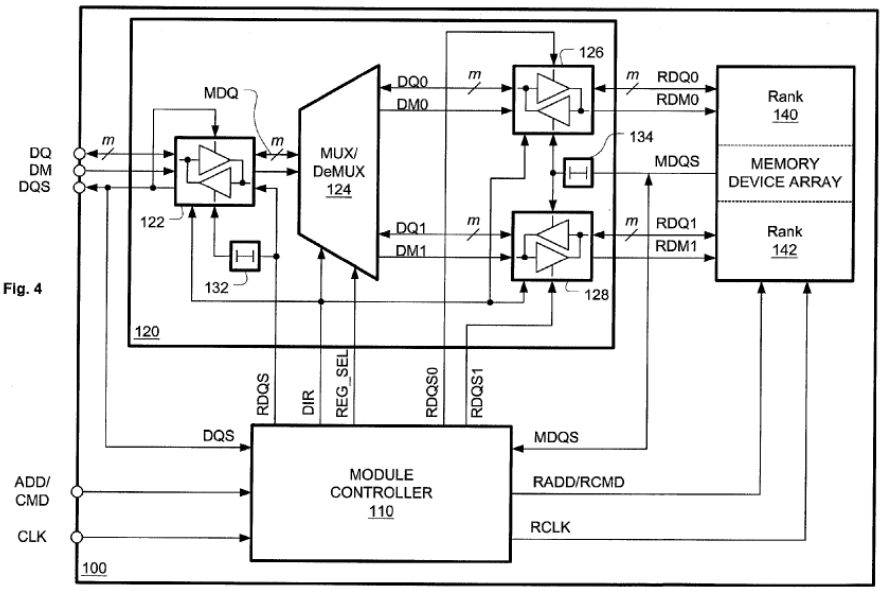


Fig. 4

Halbert, Fig. 4; Decl., ¶ 115.

Data interface circuit 120, "provides for m-bit-wide data transfers between the module and the system memory data bus, and for R×m-bit-wide data transfers

between the interface circuit and the memory device array. In Fig. 4, R=2." Halbert, [0030]; Decl., ¶ 116.

f. Limitation [1.6]

Halbert discloses Limitation [1.6]. Halbert discloses module controller 110 as logic coupled to the circuitry (data interface circuit 120). "Module controller 110 synchronizes the operation of the data port buffer 122, MUX/DeMUX 124, and data registers 126 and 128 via a number of control signals. For instance, direction signal DIR specifies whether data flow is towards the memory array (TO) or away from the memory array (AWAY)." Halbert, [0034]. When data flow is away from the memory array, module controller 110 is responding to the first memory command, i.e., read command, by providing first control signals, i.e., AWAY, to the circuitry, i.e., data interface circuit 120. Decl., ¶ 118. Similarly, when data flow is towards the memory array, module controller 110 is responding to the second memory command (write command), by providing second control signals, (TO), to the circuitry (data interface circuit 120). *Id*.

Alternatively, module controller 110 responds to the first memory command (read command), by providing first control signals (AWAY) and register select signal REG_SEL, to data interface circuit 120 to determine that DQ0 will be supplied to buffer 122 in response. "The register select signal REG_SEL, in the AWAY mode, determines whether DQ 0 or DQ1 will be supplied to buffer 122."

Halbert, [0035]. Subsequently, module controller 110 responds to the second memory command (second read command), by providing second control signals (AWAY) and register select signal REG_SEL, to data interface circuit 120, to determine that DQ1 will be supplied to buffer 122 in response. "For instance, REG_SEL can first select, e.g., DQ0 during a first bus clock cycle, and then DQ1 during the following bus clock cycle." *Id*.; Decl., ¶ 119.

g. Limitation [1.7]

Halbert discloses Limitation [1.7]. Halbert discloses that in response to the first control signals, i.e., in the AWAY mode, data transfers are enabled through data interface circuit 120 to buffer 122 toward the system memory data bus. "The register select signal REG_SEL, in the AWAY mode, determines whether DQ 0 or DQ1 will be supplied to buffer 122. Data is serialized from the data registers onto the memory data bus by reading 2m bits into the data registers during one memory device read cycle, and then driving these bits, m at a time, through MUX 124." Halbert, [0035]; Decl., ¶ 120.

Halbert further discloses that subsequently in response to the second control signals, i.e., in the TO mode, data transfers are enabled through data interface circuit 120 to registers 126 and 128 toward the memory array. "In the TO mode, REG_SEL determines which of registers 126 and 128 will receive DQ at each memory bus clock cycle (note that an alternative is to supply DQ to the inputs of both registers,

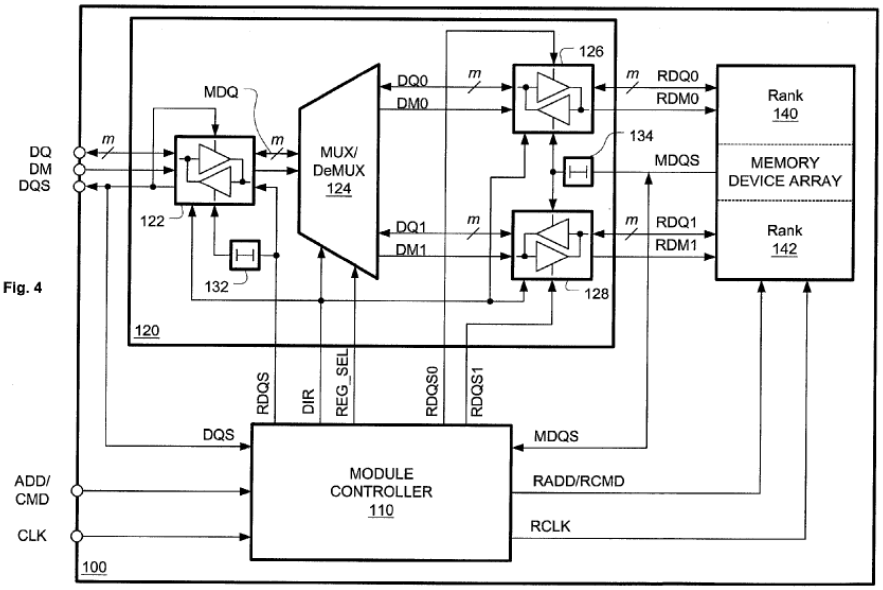
and ignore REG_SEL). … Both register contents are then written to memory device array 140/142 during a single device write cycle." Halbert, [0036]; Decl., ¶ 121.

Alternatively, data transfers are enabled through data interface circuit 120 to buffer 122 supplied by DQ0 in response to the first control signals, i.e., AWAY and REG_SEL, and then subsequently enabled through data interface circuit 120 to buffer 122 supplied by DQ1 in response to the second control signals, i.e., AWAY and REG_SEL. "The "register select signal REG_SEL, in the AWAY mode, determines whether DQ 0 or DQ1 will be supplied to buffer 122. … For instance, REG_SEL can first select, e.g., DQ0 during a first bus clock cycle, and then DQ1 during the following bus clock cycle." Halbert, [0035]; Decl., ¶ 122.

h. Limitations [1.8]-[1.9]

Halbert discloses Limitations [1.8]-[1.9]. Halbert discloses that "one embodiment describes a DIMM that can, with the same type of devices, number of devices, and data signal pins as the dual-bank registered DIMM, provide twice the data rate of the registered DIMM." Halbert, [0024]. A POSITA would have understood that Halbert's memory module 100 enables data signals and strobes transfer from the memory device array *to the system memory data bus in response to read commands*, and from the system memory data bus *to the memory device array in response to write commands*, at the specified data rate, i.e., at twice the data rate of the registered DIMM. Decl., ¶¶ 123, 125, 127; *see also* Halbert, [0035]

(describing the AWAY (read) mode); [0036] (describing the TO (write) mode). As shown in Fig. 4, the first burst of data signals and strobes are transferred through the circuitry (data interface circuit 120).



Halbert, Fig. 4 (data signals are input and output from data interface circuit 120 on RDQ0 and RDQ1, and data strobes are input and output from data interface circuit 120 on MDQS); *see also id.*, [0030]-[0031], [0038]; Decl., ¶¶ 124, 126.

i. Limitation [1.10]

Halbert discloses Limitation [1.10]. As shown in Fig. 4, Halbert discloses registers 126, 128, and 122 for providing registered data transfers through data interface circuit 120.

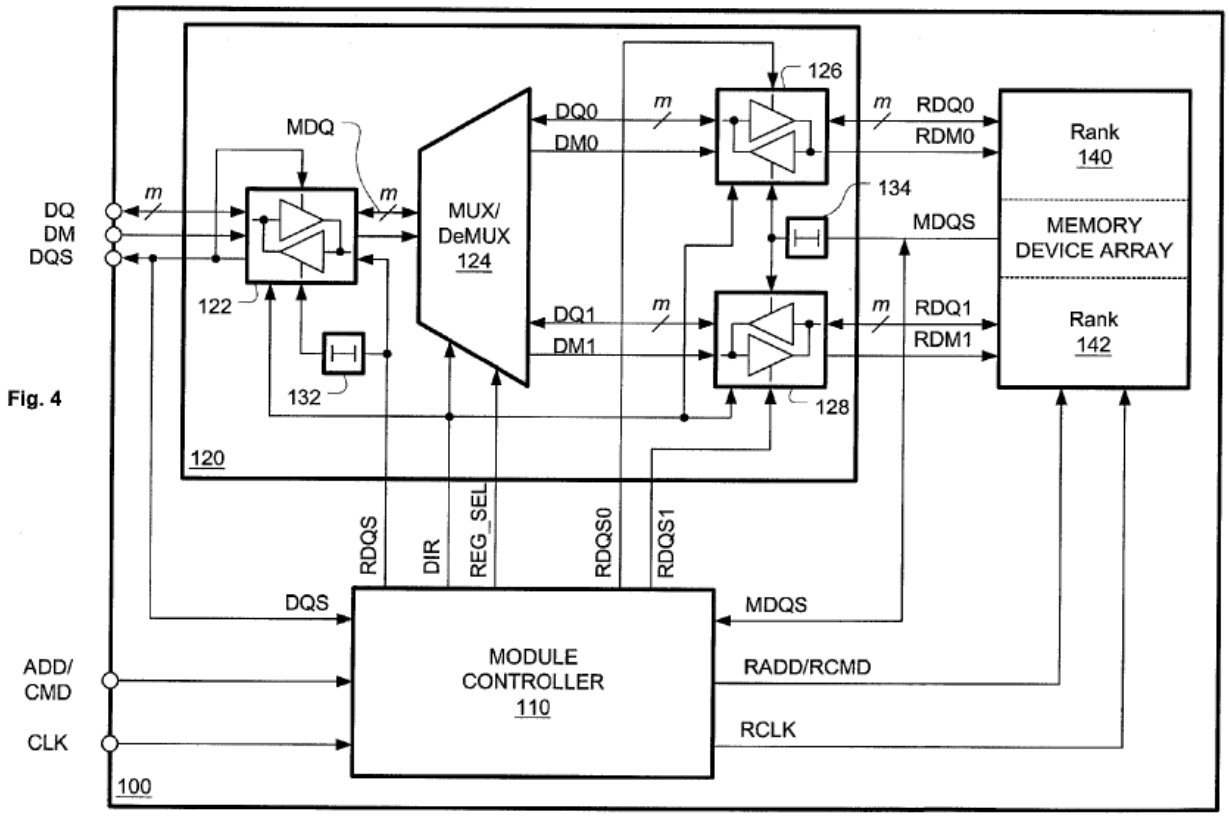


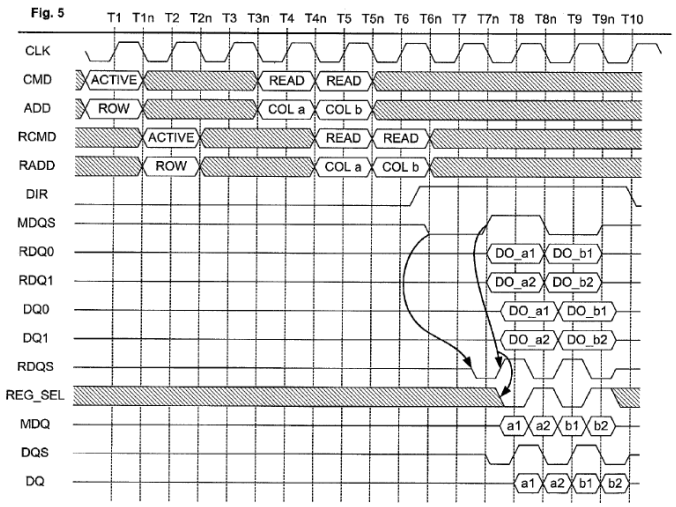
Fig. 4

Halbert, Fig. 4. Halbert discloses that "either data signals DQ0 (from register 126) or data signals DQ1 (from register 128) can be multiplexed to buffer 122 when the module is reading from memory device array 140/142." *Id*., [0033]. Likewise, "[i]n the TO mode, REG_SEL determines which of registers 126 and 128 will receive DQ at each memory bus clock cycle." *Id*., [0036]; Decl., ¶ 129.

Moreover, Halbert discloses that the registered data transfers are enabled by module controller 110 *in accordance with an overall CAS latency* of memory module 100. "The module controller 110 synchronizes the operation of module 100 with the attached memory system. Like the address/command registers and PLL of a registered DIMM, controller 110 can provide clock adjustment to an input CLK

signal … In addition, module controller 110 provides timing and synchronization signals to data interface circuit 120." Halbert, [0029]. A POSITA would have understood that module controller 110 provides all the necessary signals to synchronize the operation of memory module 100, including in accordance with the overall CAS latency of memory module 100. Decl., ¶ 130. In other words, a POSITA would have understood that because the data transfers occur within a timespan that would be considered the overall CAS latency of the memory module, the data transfers are enabled in accordance with the overall CAS latency of the memory module. *Id*.

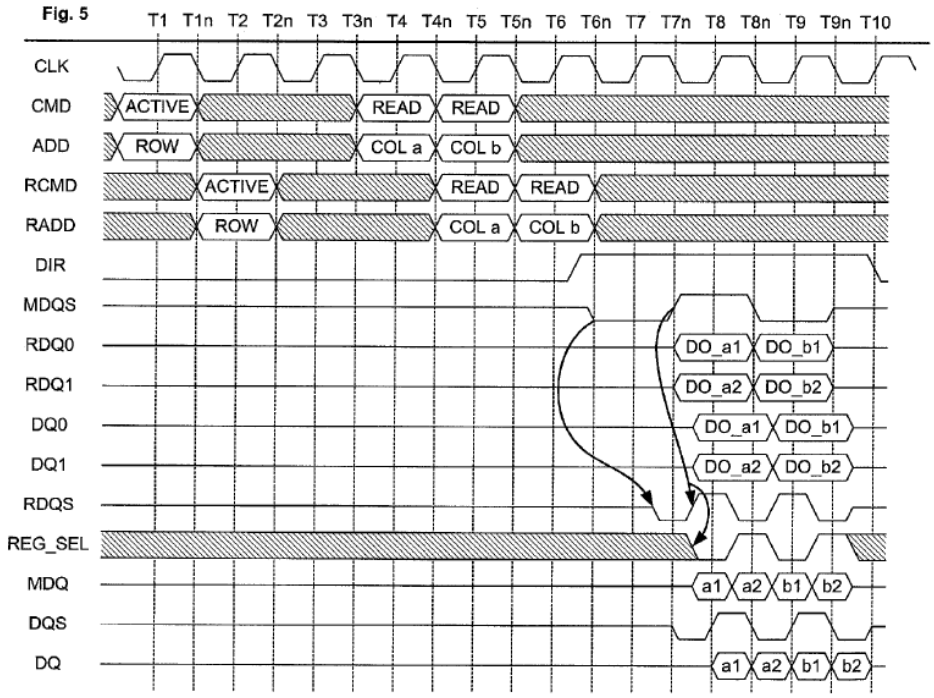
Halbert's Fig. 5 depicts a timing diagram for two consecutive read operations for the memory module of FIG. 4. The READ command for COL a is clocked in at T4 and data a1 and a2 are available on DQ at T8 and T8n, respectively. The registered data transfers DO_a1 and DO_a2 are enabled on RDQ0 and RDQ1 at T7n. Thus, Fig. 5 shows that the registered data transfers (which happen at T7n) are enabled within the overall CAS latency of memory module 100, i.e., T4 to T8.



Halbert, Fig. 5; Decl., ¶ 131. This meets both sides' proposed construction of "overall CAS latency of the memory module" because T4 to T8 is the "the delay between: (1) the time when a command is executed/sampled on the memory module [the READ command for COL a clocked in at T4], and (2) a time when the first piece of data is available at the output/data pins of the memory module [data a1 available on DQ at T8]." Decl., ¶ 131.

j. Limitation [1.11]

Halbert discloses Limitation [1.11]. Referring again to Fig. 5, data interface circuit 120 is configured to add a predetermined amount of time delay for each registered data transfer through the circuitry because registers 126 and 128 add a predetermined time delay of one clock cycle for each registered data transfer through circuit 120.



Halbert, Fig. 5; Decl., ¶ 132. Data transfers through the memory module begin with the READ command of COL a clocked in at T4 and of COL b clocked in at T5, respectively. Registers 126 and 128 of the data interface circuit 120 each add a one clock cycle delay to data transfers through circuit 120, as shown, e.g., by the one clock cycle delay between the time when register 126 latches a first piece of data (DO_a1) onto bus DQ0 (from bus RDQ0) and the time when register 126 latches the next piece of data (DO_b1) onto bus DQ0 (from bus RDQ0). As a result, the overall CAS latency of memory module 100, e.g., from T4 to T8, is greater than the actual operational CAS latency of each of the plurality of memory integrated circuits, e.g., from T5 to T7n (where the memory device array makes the data available on RDQ0). *Id*. A POSITA would understand that "[i]n a registered DIMM, data is delayed an

additional clock cycle due to the on-DIMM pipeline register (that is, Device CL [clock cycles] + 1 = DIMM CAS latency." JESD21-C, 68; Decl., ¶ 133. This meets both sides' proposed construction of "actual operational CAS latency of each of the memory devices" because T4 to T8 is greater than "the delay between: (1) the time when a command is executed by each of the plurality of memory devices [the registered READ command for COL a clocked in at T5], and (2) a time when the first piece of data is available at the output/data pins of each of the plurality of memory devices [where the data exits the memory device array on RDQ0] at T7n." Decl., ¶ 132.

2. Claim 2

a. Limitation [2.1]

Claim 2 depends on claim 1. The '314 patent states "[a]s used herein, the term 'load' is a broad term which includes, without limitation, electrical load, such as capacitive load, inductive load, or impedance load." Ex. 1001, 6:1-3.

Halbert discloses Limitation [2.1]. Halbert discloses that "[t]he exemplary embodiments also allow the memory devices to be isolated from the full capacitive loading effects of the system memory data bus." Halbert, [0024]. Halbert further discloses that "[t]wo bi-directional data registers 126 and 128 connect, respectively, to memory device array ranks 140 and 142. Each data register can receive an m-bit-wide word from its corresponding memory device rank, or drive an m-bit-wide word

to that rank, over a dedicated point-to-point module data bus." *Id*., [0032]. A POSITA would have understood that each of the plurality of memory integrated circuits (memory device ranks 140 and 142), has a corresponding load (the capacitive loading of RDQ0 and RDQ1 transfers to and from registers 126 and 128, respectively). Decl., ¶¶ 136-137. "[T]he number of device inputs also determine the capacitance that a memory device (or the controller) sees when it drives the bus." Halbert, [0025]. Thus, the m RDQ lines each has its own associated capacitive loading. Decl., ¶ 137.

b. Limitation [2.2]

Halbert discloses Limitation [2.2]. Halbert discloses that "[t]he memory systems and modules described herein generally improve upon the multi-drop memory bus architecture by isolating the memory devices on each module from the bus." Halbert, [0026]. Moreover, "[t]he exemplary embodiments also allow the memory devices to be isolated from the full capacitive loading effects of the system memory data bus." *Id*., [0024]. As depicted in Fig. 4, the circuitry of circuit 120, e.g., multiplexer/demultiplexer (MUX/DeMUX) 124, bi-directional buffer 122, and bi-directional data registers 126 and 128, isolates the loads of the plurality of memory integrated circuits, i.e., the capacitive loading of RDQ0 and RDQ1, from the memory controller (to the left of Fig. 4), i.e., the input/output on DQ. Decl., ¶ 138.

3. Claim 6

Claim 6 depends on claim 1. Halbert discloses the limitation of Claim 6. Data transfer through register 126 is one pipeline and through register 128 is a second pipeline. Halbert discloses that "either data signals DQ0 (from register 126) or data signals DQ1 (from register 128) can be multiplexed to buffer 122 when the module is reading from memory device array 140/142. Likewise, when the module is writing to the memory device array, data signals MDQ from buffer 122 can be channeled to either DQ0 or DQ1." Halbert, [0033]. Thus, Halbert discloses that data interface circuit 120 includes logic pipelines, i.e., the circuit paths from buffer 122 through MUX/DeMUX 124 through either register 126 or register 128, that enable data transfers through the circuitry in response to the first control signals associated with the read operation, and subsequently in response to the second control signals associated with the write/second read operation. Decl., ¶¶ 140-142.

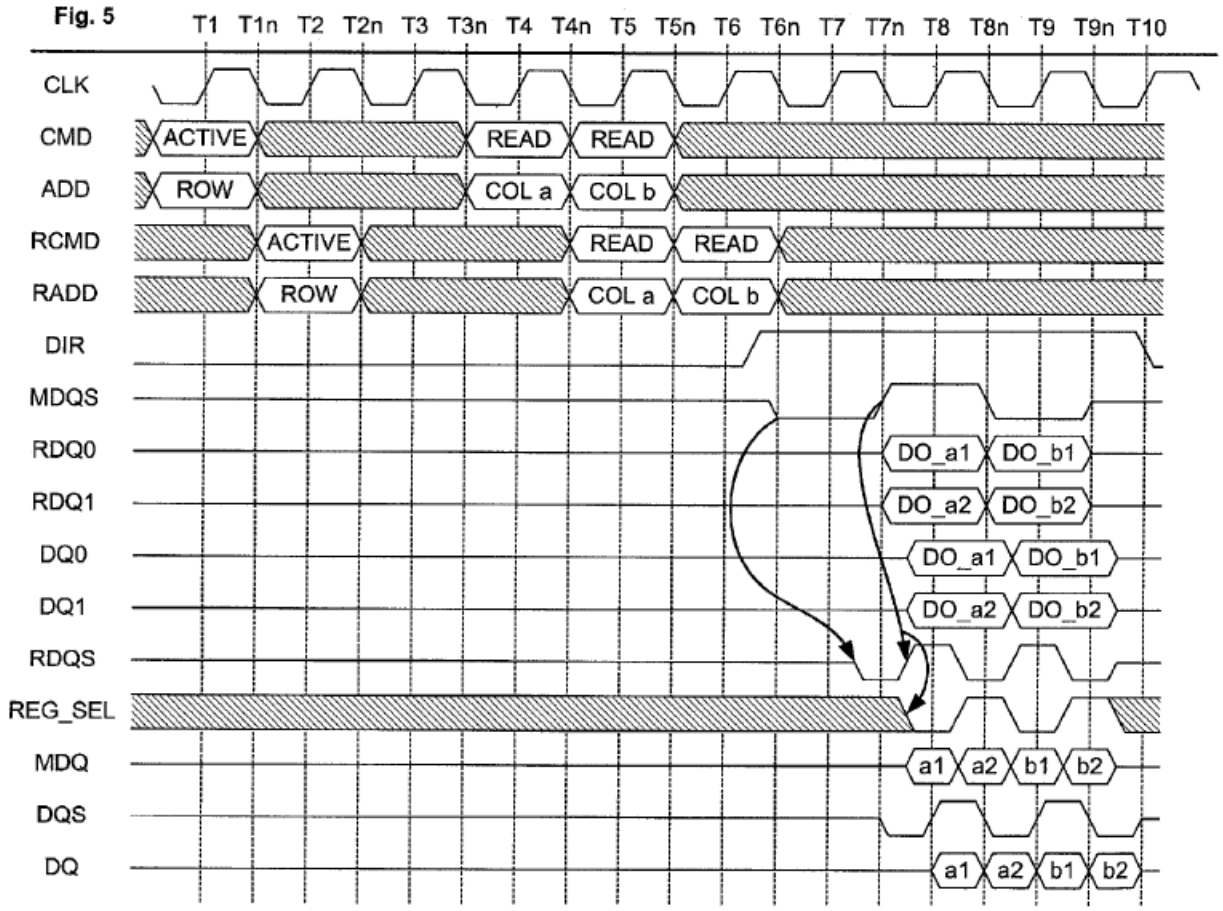
4. Claim 8

Claim 8 depends on claim 1. Halbert discloses the limitation of Claim 8. Halbert discloses that "[i]n one embodiment, the memory module has two ranks of memory devices, each rank connected to a corresponding one of two 64-bit-wide data registers." Halbert, Abstract. Thus, Halbert discloses N-bit wide as 64-bit-wide. Decl., ¶¶ 144-145.

5. Claim 12

a. Limitation [12.1]

Claim 12 depends on claim 1. Halbert discloses Limitation [12.1]. Fig. 5 of Halbert "illustrates a timing diagram for two consecutive read operations (to the same ROW of the memory devices)." Halbert, [0037]. The read operation provides the first burst of N-bit wide data signals and data strobes that are transferred through data interface circuit 120 during time intervals of a first plurality of time intervals, as shown below.

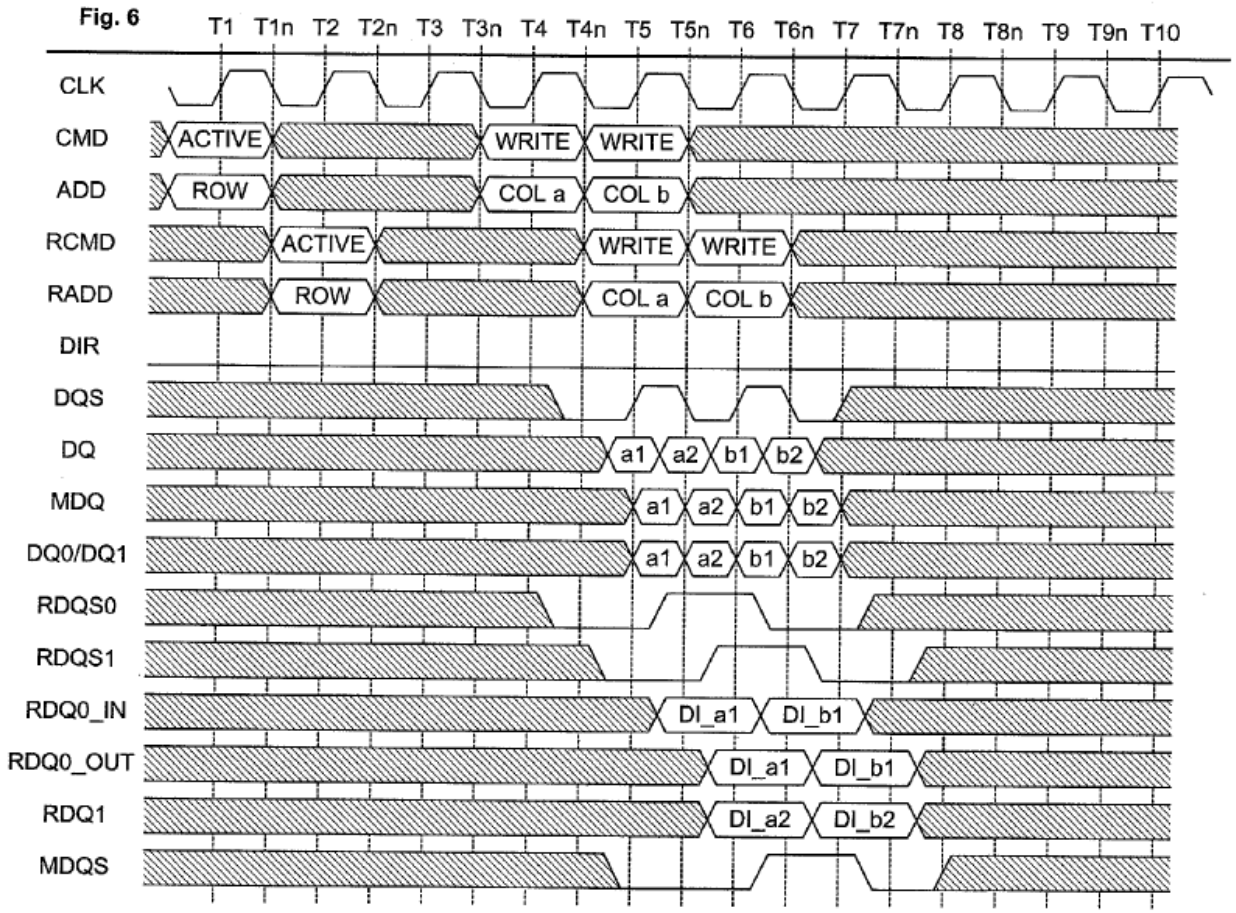


Id., Fig. 5; Decl., ¶¶ 147-148.

Referring to Fig. 5, Halbert discloses that "[a]pproximately a half-clock cycle after transitioning RDQS and REG#_SEL, controller 110 transitions these signals again to place DO_a2 on the memory bus. While DO_a2 is being latched into buffer 122 (at T8n), the memory devices begin data output of the results of the second READ operation. The results of the second read operation propagate through the interface circuit in similar fashion to the results of the first read operation." Halbert, [0042]. Thus, as shown in Fig. 5, the respective N-bit wide data signals of the first burst of N-bit wide data signals DO_a1 and DO_b1 and the respective data strobes of the first burst of data strobes MDQS are transferred through the circuitry during respective time intervals of a first plurality of time intervals, e.g., at least the time interval that includes the time from T8 to T9. Decl., ¶ 149.

b. Limitation [12.2]

Halbert discloses Limitation [12.2]. Fig. 6 of Halbert "shows an analogous [to Fig. 5] timing diagram for two consecutive write operations." Halbert, [0043]. The write operation provides the second burst of N-bit wide data signals and data strobes that are transferred through data interface circuit 120 during time intervals of a second plurality of time intervals, as shown below.



Id., Fig. 6; Decl., ¶ 150.

Halbert discloses that "[i]n one memory bus clock cycle, m bits are directed to register 126 by strobing RDQS0. In the following bus clock cycle, m bits are directed to register 128 by strobing RDQS1. … Controller 110 strobes the memory device array, using the memory data strobe MDQS, to signal the array to write data from buses RDQ0 and RDQ1." Halbert, [0046]. Thus, as shown in Fig. 6, the respective N-bit wide data signals of the second burst of N-bit wide data signals DI_a2 and DI_b2 and the respective data strobes of the second burst of data strobes MDQS are transferred through the circuitry during respective time intervals of a

second plurality of time intervals, e.g., at least the time interval that includes the time from T6 and T7. Decl., ¶ 151.

6. Claim 13

a. Limitation [13.1]

Claim 13 depends on claim 1. Halbert discloses Limitation [13.1]. Halbert discloses that "[i]n a registered DIMM, the system clock CK0 is received by phase-locked-loop (PLL) 27, which creates a set of module clock signals." Halbert, [0009]. The system clock CK0 signal is sent from the memory controller to the PLL, which in response, outputs a set of module clock signals. Decl., ¶¶ 153-154.

Halbert further discloses that "a primary memory controller initiates READ operations [for memory module 100] just like it would for a registered DIMM." Halbert, [0037]. Memory Module 100 is just another design of a registered DIMM. Thus, it would have been obvious to have the memory controller send the system clock CK0 to a PLL to output clock signals, i.e., a set of module clock signals, for memory module 100. Decl., ¶ 155.

b. Limitation [13.2]

Halbert discloses Limitation [13.2]. As discussed above for Limitation [1.11], Halbert discloses that data interface circuit 120 is configured to add a predetermined time delay of one clock cycle for each registered data transfer. *See* §V.B.1.j. It would have been obvious to a POSITA that registers 126 and 128 could each be configured to add a one clock cycle time delay. *See, e.g.*, Halbert, [0010] (Signals

pass through a register with a one clock cycle time delay. "Register 25 latches these signals, and places them on the module bus at T2. After a known RAS (row address strobe) latency, the controller transmits a READ command along with a COL 'a' address. These signals also pass through register 25 with a one-clock cycle delay."); *see also* JESD21-C, 68; Decl., ¶ 156.

7. Claim 14

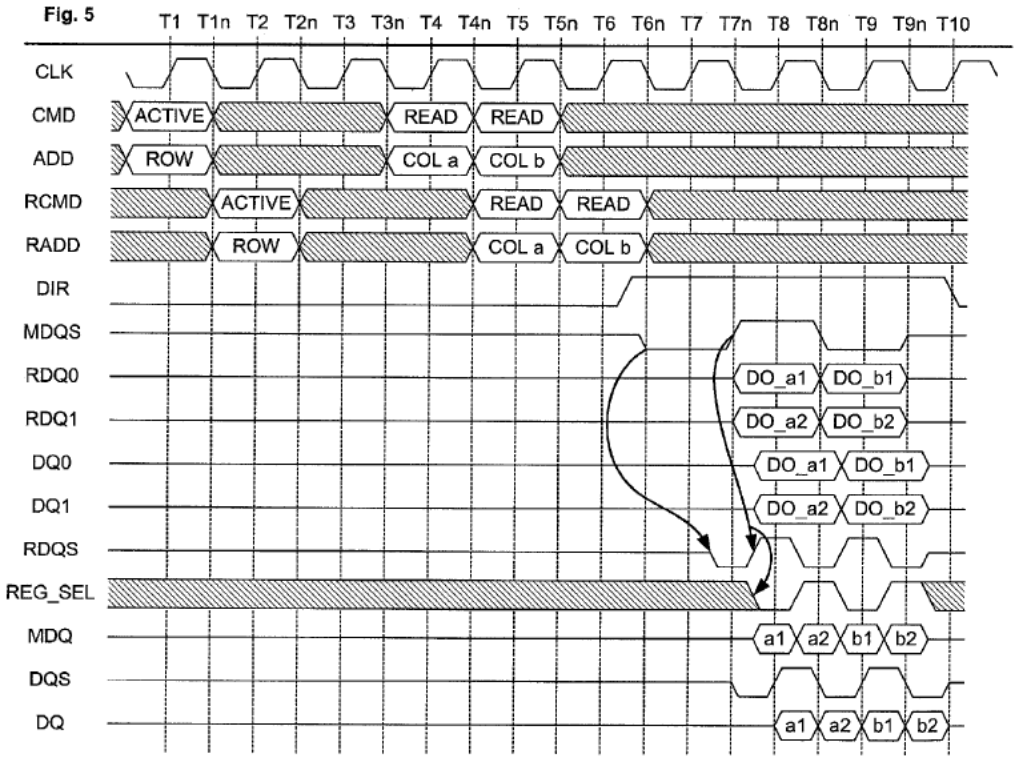
a. Limitation [14.1]

Claim 14 depends on claim 13. Halbert discloses Limitation [14.1]. Halbert discloses that the "types, sizes, or numbers of memory devices selected for use with the present invention are not critical. Some possible device types include dynamic random access memory (DRAM) devices, *synchronous DRAM (SDRAM) devices*." Halbert, [0061] (emphasis added). Moreover, Halbert discloses that the SDRAM is configured to operate synchronously with the clock signal by the module controller 110. "The module controller 110 synchronizes the operation of module 100 with the attached memory system." *Id*., [0029]. Decl., ¶¶ 158-159.

b. Limitation [14.2]

Halbert discloses Limitation [14.2]. Halbert discloses that "[d]evice array 140/142 signifies that it is about to drive data onto buses RDQ0 and RDQ1 by taking data strobe MDQS low at T6n." Halbert, [0038]. Thus, device array 140 is configured to output data onto bus RDQ0. Decl., ¶ 160.

The data is output on both edges of the respective set of data strobes of the first burst of data strobes. Referring to Fig. 5 below, the first burst of N-bit wide data signals from memory device 140, i.e., DO_a1 and DO_b1, is output onto RDQ0 at T7n and T8n, respectively. DO_a1 is output on the rising edge of the respective set of data strobes of the first burst of data strobes, i.e., MDQS, at T7n, and DO_b1 is output on the falling edge of MDQS at T8n.



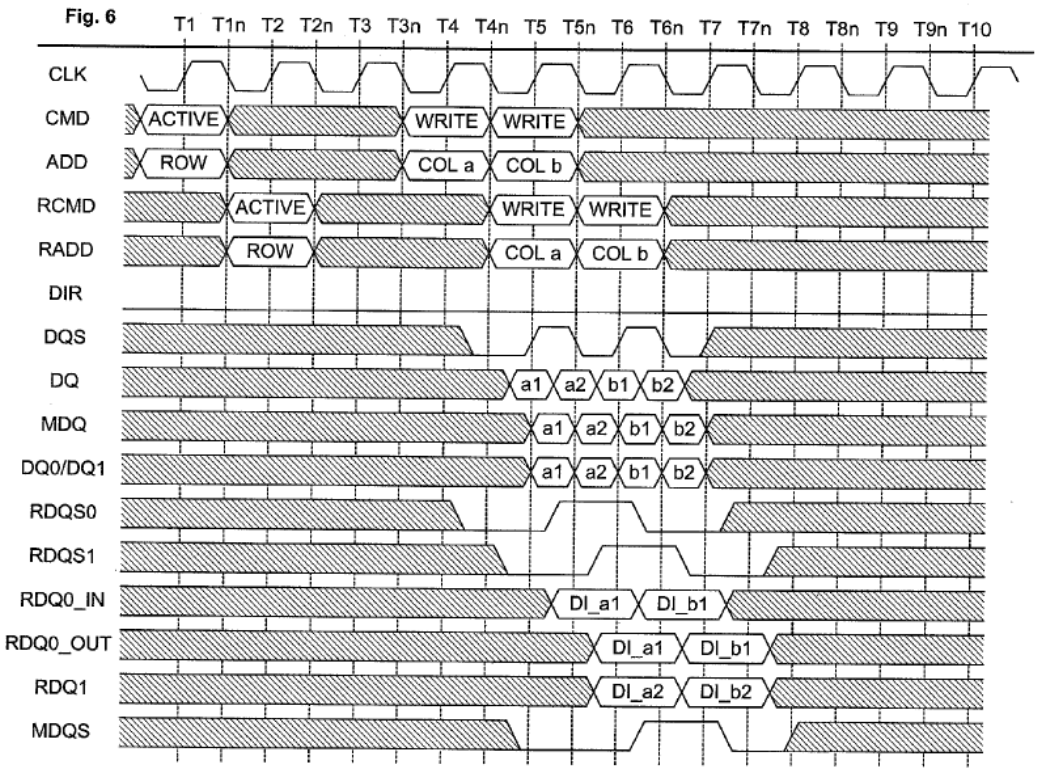
Id., Fig. 5; Decl., ¶ 161.

c. Limitation [14.3]

Halbert discloses Limitation [14.3]. Halbert discloses that "[c]ontroller 110 strobes the memory device array, using the memory data strobe MDQS, to signal the

array to write data from buses RDQ0 and RDQ1." Halbert, [0036]. Thus, device array 142 is configured to receive data from bus RDQ1. Decl., ¶ 162.

The data is received on both edges of the respective set of data strobes of the second burst of data strobes. Referring to Fig. 6 below, the second burst of N-bit wide data signals received by memory device 142, i.e., DI_a2 and DI_b2, is ready on bus RDQ1 a quarter clock cycle after T5n and a quarter clock cycle after T6n, respectively. DI_a2 is received by memory device 142 on the rising edge of the respective set of data strobes of the second burst of data strobes, i.e., MDQS, at a quarter clock cycle after T6, and DI_b2 is received by memory device 142 on the falling edge of MDQS at a quarter clock cycle after T7.



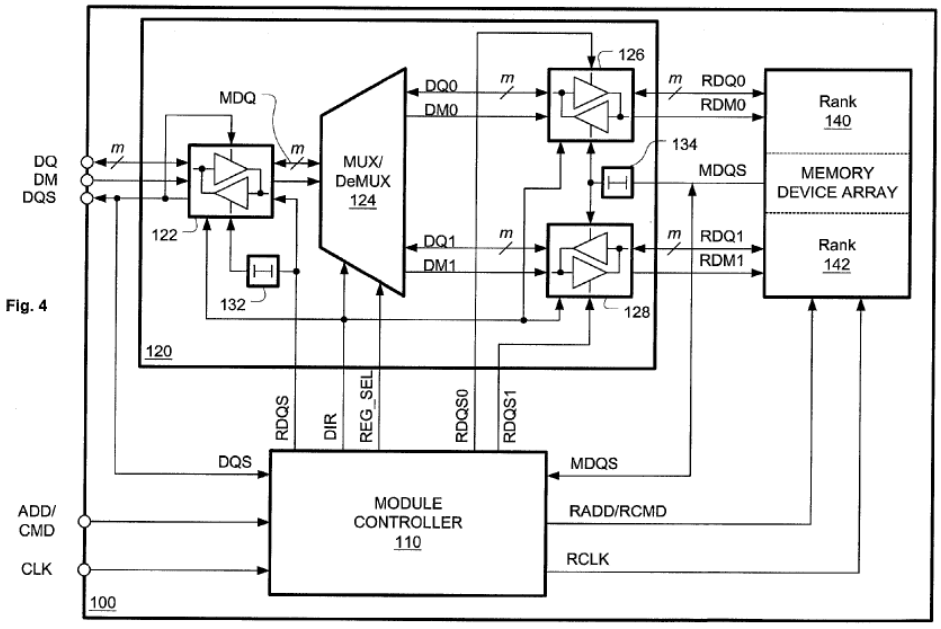
Id., Fig. 6; Decl., ¶ 163.

C. Ground 2: Halbert in View of JESD21-C Render Claims 3 and 9-10 Obvious

1. Claim 3

a. Limitations [3.1]-[3.2]

Claim 3 depends on claim 1. Halbert discloses Limitations [3.1]-[3.2]. As explained for Limitations [1.2] and [1.6], the logic, module controller 110, is coupled to the circuit board, and "can provide … registered versions of address and command signals, RADD/RCMD." Halbert, [0029]. Specifically, "[a]ddress and command signals ADD/CMD are latched into a register 25 at the edge of one clock cycle, and then redriven onto the module addressing/command bus as register signals RADD/RCMD." *Id*., [0009]. This happens in module controller 110 shown in Fig. 4.

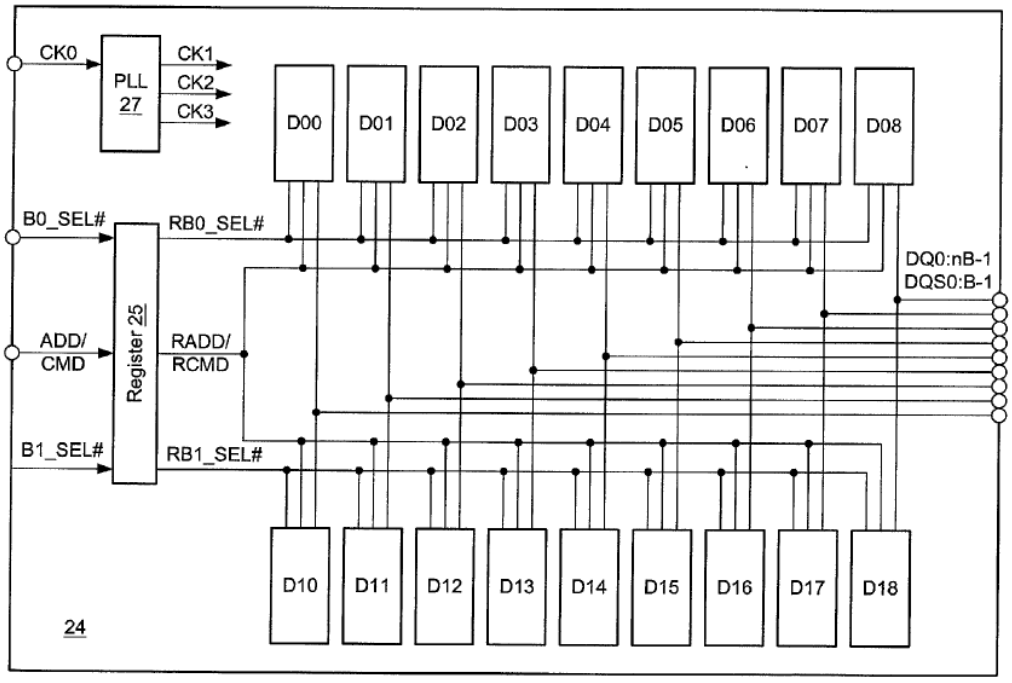


Halbert, Fig. 4; Decl., ¶¶ 165-167. Fig. 4 shows a first set of input address and control signals (ADD/CMD), which is associated with the first memory command (read command), input into module controller 110 and a first set of registered address and control signals (RADD/RCMD), output from the module controller 110. *See also id*., Fig. 5 (showing RCMD and RADD); Decl., ¶ 167. The same process occurs for read commands, i.e., the first memory command, write commands, i.e., the second memory command, and even subsequent read/write commands, i.e., another second memory command. Halbert, [0037], Fig. 6 (a timing diagram for two consecutive write operations); Decl., ¶¶ 168-169.

b. Limitations [3.3]-[3.4]

Halbert discloses Limitations [3.3]-[3.4]. In describing registered DIMM designs, as depicted in Fig. 2 below, Halbert discloses that there are "two bank select signals, B0_SEL# and B1_SEL#, each pass[ing] through register 25 and connect[ing] to a chip select pin on a corresponding one of the banks of memory devices." Halbert, [0009].

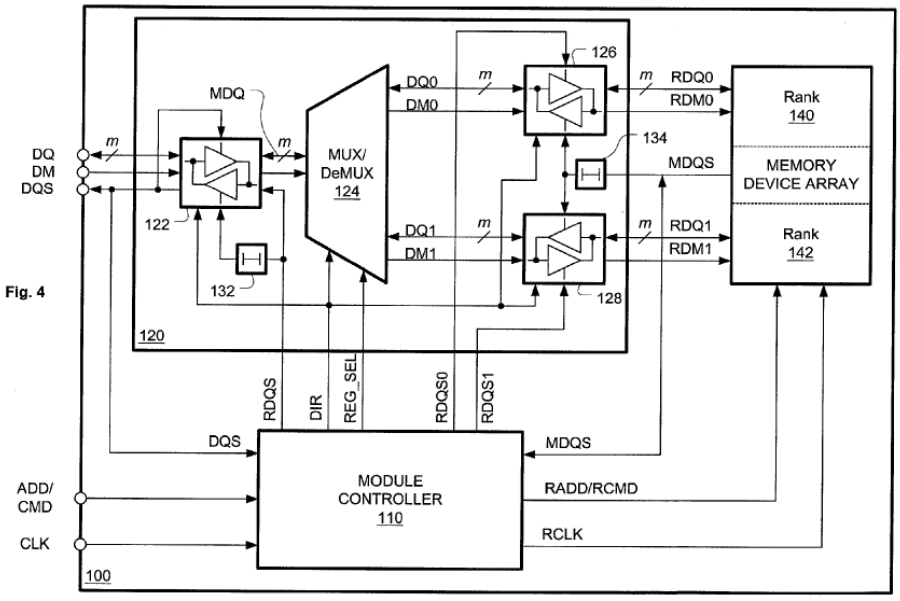
Fig. 2
(Prior Art)



Id., Fig. 2. B0_SEL# and B1_SEL# are a first and second set of input chip select signals corresponding to the D00-D08 and D10-D18 memory ranks, respectively, and are part of the first and second set of input address and control signals (ADD/CMD). Decl., ¶¶ 170, 177.

Referring to Fig. 4, it would have been obvious to a POSITA to include the first and second set of input chip select signals B0_SEL# and B1_SEL# with the ADD/CMD signals sent by the same memory controller to module controller 110, similar to B0_SEL# and B1_SEL# input to register 25 in Fig. 2, to correspond to memory device ranks 140 and 142, respectively, because Halbert discloses, e.g., "a primary memory controller initiates READ operations [for memory module 100] just like it would for a registered DIMM." Halbert, [0037]. Memory Module 100 is

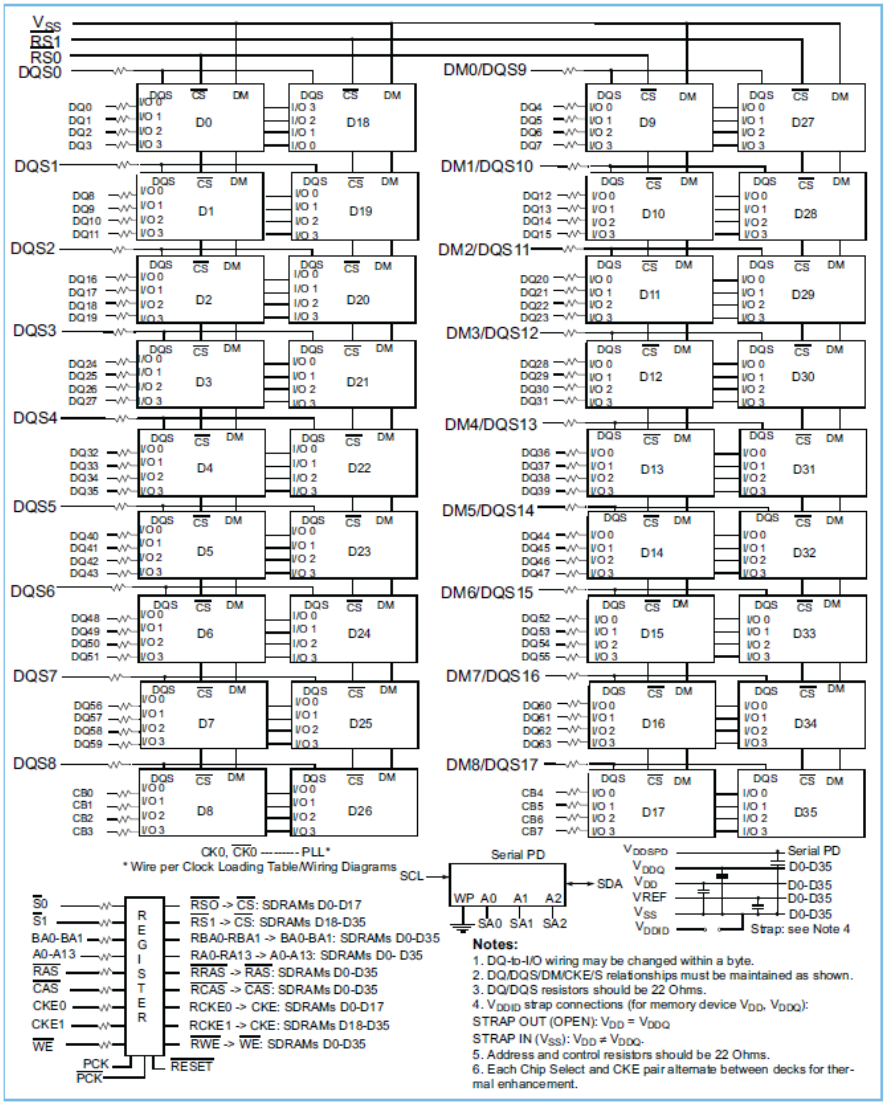
just another design of a registered DIMM, so it would have been obvious to include B0_SEL# and B1_SEL# with the ADD/CMD signals of Fig. 4. Module controller 110 in Fig. 4 would have a set of chip selects as inputs because there are multiple memory device ranks 140 and 142, and there would be chip selects to select whether data is transferred to/from memory device rank 140 or 142.



Id., Fig. 4; Decl., ¶¶ 171, 178.

To the extent Halbert does not teach this limitation, it would have been obvious in view of JESD21-C. JESD21-C discloses a first and second set of input chip select signals S0 and S1 input to the register, as shown in Block Diagram: Raw Card Version N ("Card N") below. Chip select S0 corresponds to the rank that includes the D0-D17 memory devices, and chip select S1 corresponds to the rank that includes the D18-D35 memory devices.

Block Diagram: Raw Card Version N (Populated as two physical banks of x4 DDR SDRAMs)



JESD21-C, 15; Decl., ¶¶ 172, 179. JESD21-C's Card N discloses a block diagram of two physical banks of x4 DDR SDRAMs, which is what is disclosed in Fig. 4 of Halbert, i.e., memory device ranks 140 and 142. Thus, like Fig. 2 in Halbert, there would be a first and second set of chip selects input to module controller 110 in Fig. 4. *Id*.

Furthermore, a POSITA would have been motivated to combine the teachings of Halbert with JESD21-C because both references are in the same field and directed toward solving the same problem, i.e., improving the design of memory modules that use SDRAM. Decl., ¶ 173. More specifically, a POSITA would have been motivated to design memory modules and DDR SDRAMs, such as those disclosed in Halbert, to be in compliance with an industry-wide governing standard such as JEDEC. *Id*. A POSITA would have understood that modifying Halbert's memory module 100 shown in Fig. 4 with the teachings of JESD21-C would have been obvious because Halbert is directed to "memory module configurations and access methods … [that] can improve on the dual-bank registered DIMM in several respects" (Halbert, [0024]), and JESD21-C is a specification that "defines the electrical and mechanical requirements for … 64/72 bit-wide, Registered Double Data Rate Synchronous DRAM Dual In-Line Memory Modules (DDR SDRAM DIMMs)" (JESD21-C, 5). Decl., ¶ 173. Thus, both references are directed to achieving the same goal, and a POSITA would have been motivated to incorporate any additional standardized DDR SDRAM DIMMs design requirements into Halbert's memory module 100. *Id*.

Moreover, JESD21-C is a specification for specifying the architecture for different DDR SDRAM DIMMs.

Product Family Attributes

DIMM organization	x72 ECC, x64
DIMM dimensions (nominal)	5.25" x 1.2"/1.7"
Pin count	184
SDRAMs supported	64Mb, 128Mb, 256Mb, 512Mb, 1Gb
Capacity	64MB, 128MB, 256MB, 512MB, 1GB, 2GB, 4GB
Serial PD	Consistent with JC 42.5 Rev 0
Voltage options	2.5 volt (V_{DD}/V_{DDQ})
Interface	SSTL_2

JESD21-C, 5; Decl., ¶ 174. This is the exact type of memory device that is disclosed in Halbert. "Some possible device types include dynamic random access memory (DRAM) devices, synchronous DRAM (SDRAM) devices including double-data-rate (DDR) SDRAM devices, quad-data-rate (QDR) SDRAM devices, Rambus™ DRAM devices (with an appropriate controller), static RAM and flash memory devices." Halbert, [0061]; Decl., ¶ 174. And the basic architecture of memory module 100 of Halbert is the same as some of the memory architectures described in JESD21-C. *See, e.g.*, Halbert, Fig. 4 (showing two memory ranks, 140 and 142, in the memory device array) and JESD21-C, 15 (showing Card N with two memory ranks, D0-D17 and D18-D35); Decl., ¶ 174.

Further, both Halbert's memory module 100 and the SDRAM DDR DIMM designs disclosed in JESD21-C implement similar prior art functional designs for memory devices. Decl., ¶ 175. For example, memory module 100's data interface circuit 120 in Halbert and the SDRAM DDR DIMM designs disclosed in JESD21-C both include registers to add a predetermined time delay of one clock cycle for each registered data transfer through the memory module's circuitry. *See, e.g.*,

Halbert, Fig. 5 (showing a one clock cycle delay between the time when register 126 latches a first piece of data (DO_a1) onto bus DQ0 and when it latches the next piece of data (DO_b1) onto bus DQ0) and JESD21-C, 68 ("In a registered DIMM, data is delayed an additional clock cycle due to the on-DIMM pipeline register (that is, Device CL [clock cycles] + 1 = DIMM CAS latency)."); Decl., ¶ 175. And both Halbert and JESD21-C disclose the use of chip selects to select different memory ranks. *See, e.g.*, Halbert, [0009] ("Note that two bank select signals, B0_SEL# and B1_SEL#, each pass through register 25 and connect to a chip select pin on a corresponding one of the banks of memory devices.") and JESD21-C, 15 (showing chip select signal S0 corresponding to the D0-D17 memory devices and S1 corresponding to the D18-D35 memory devices); Decl., ¶ 175.

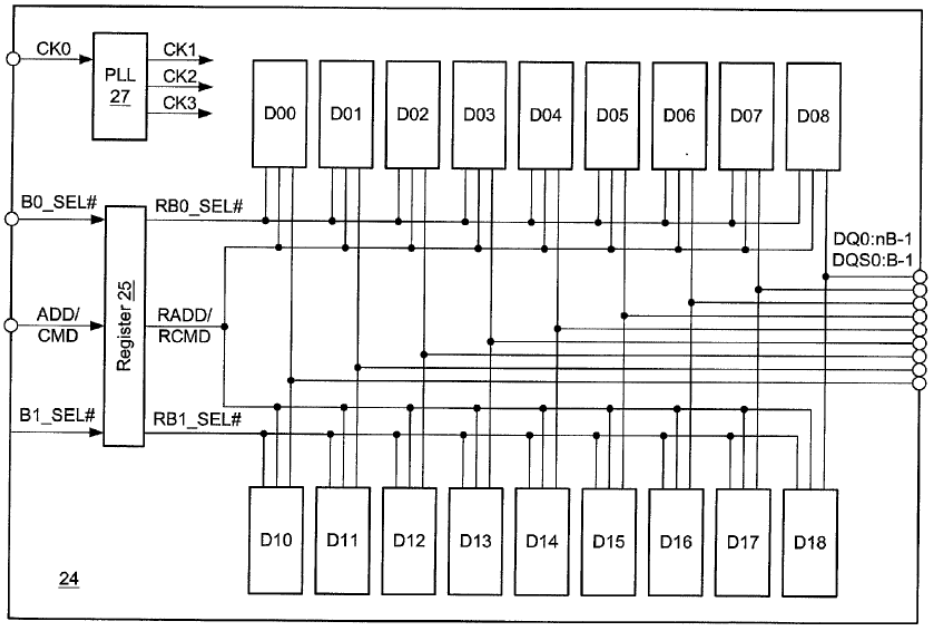
Applying the teachings of JESD21-C to Halbert would not have been beyond the skill of a POSITA and would follow the typical course of technological progression. Decl., ¶ 176. A POSITA would have understood that the number and configuration of ranks and memory integrated circuits in a memory module, as well as the use of chip selects for selecting memory ranks and registers for data transfers, are design choices. *Id*. Accordingly, modifying Halbert's memory module 100 to incorporate one of the many different DDR SDRAM architectures and features disclosed in the contemporaneous JESD21-C would have been obvious. *Id*. Indeed, Halbert contemplates different DDR SDRAM architectures. "The data lines DQ of

the memory device banks each connect to the memory bus of the host system. A total of nB DQ lines carry data signals, where B is the number of devices in one bank (e.g., eight or nine), and n is the data width of each device (e.g., four, eight, or sixteen bits)." Halbert, [0009]. Such a modification would also have been obvious because it was one of a finite number of solutions, not beyond the skill of an ordinary artisan to implement, and would have yielded predictable results. Decl., ¶ 176. Thus, a POSITA would have been motivated to incorporate the teachings of JESD21-C into the memory system of Halbert. *Id*.

c. Limitations [3.5]-[3.6]

Halbert discloses Limitations [3.5]-[3.6]. Halbert discloses that the "two bank select signals, B0_SEL# and B1_SEL#, each pass through register 25 and connect to a chip select pin on a corresponding one of the banks of memory devices." Halbert, [0009]. Thus, along with the first and second sets of registered address and control signals, i.e., RADD/RCMD, Halbert discloses RB0_SEL# and RB1_SEL# as a first and second plurality of registered chip select signals that correspond to the first and second plurality of input chip select signals, i.e., B0_SEL# and B1_SEL#, respectively, as shown in Fig. 2 below.

Fig. 2
(Prior Art)



Id., Fig. 2; Decl., ¶¶ 181, 185.

Referring to Fig. 4 below, it would have been obvious to a POSITA to include the first and second plurality of registered chip select signals RB0_SEL# and RB1_SEL# that correspond to the first and second plurality of input chip select signals B0_SEL# and B1_SEL#, respectively, with the RADD/RCMD signals output by module controller 110, similar to RB0_SEL# and RB1_SEL# output from register 25 in Fig. 2, because Halbert discloses, e.g., "a primary memory controller initiates READ operations [for memory module 100] just like it would for a registered DIMM." Halbert, [0037]; Decl., ¶¶ 182, 186. Memory Module 100 is just another design of a registered DIMM, so it would have been obvious to include RB0_SEL# and RB1_SEL# with the RADD/RCMD signals of Fig. 4. *Id*. Module controller 110 in Fig. 4 would have a plurality of registered chip selects as outputs

because there are multiple memory device ranks 140 and 142, and there would be registered chip selects to select whether data is transferred to/from memory device rank 140 or 142.

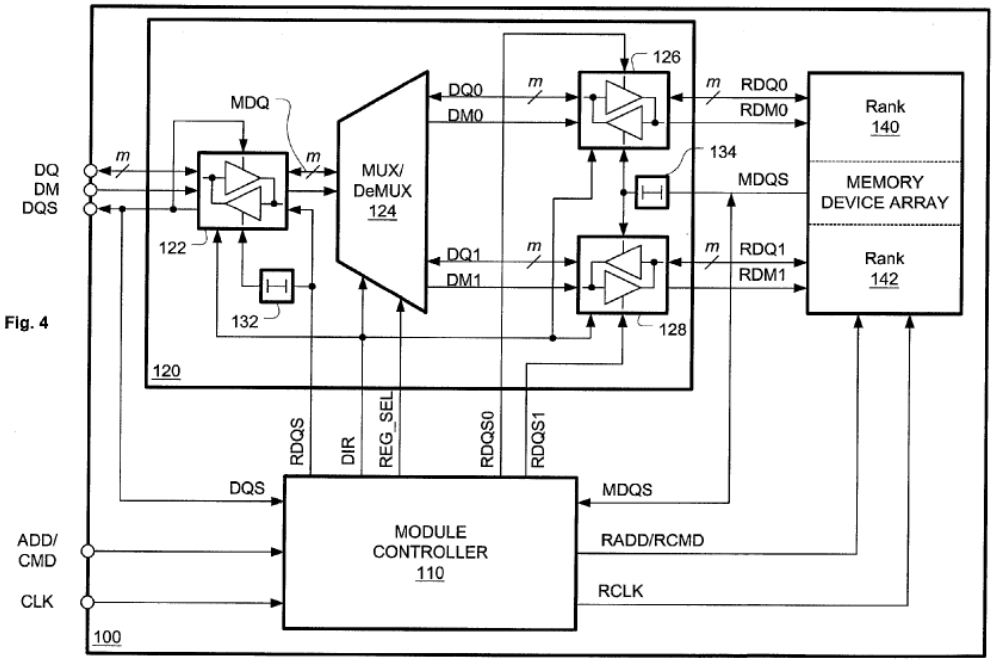
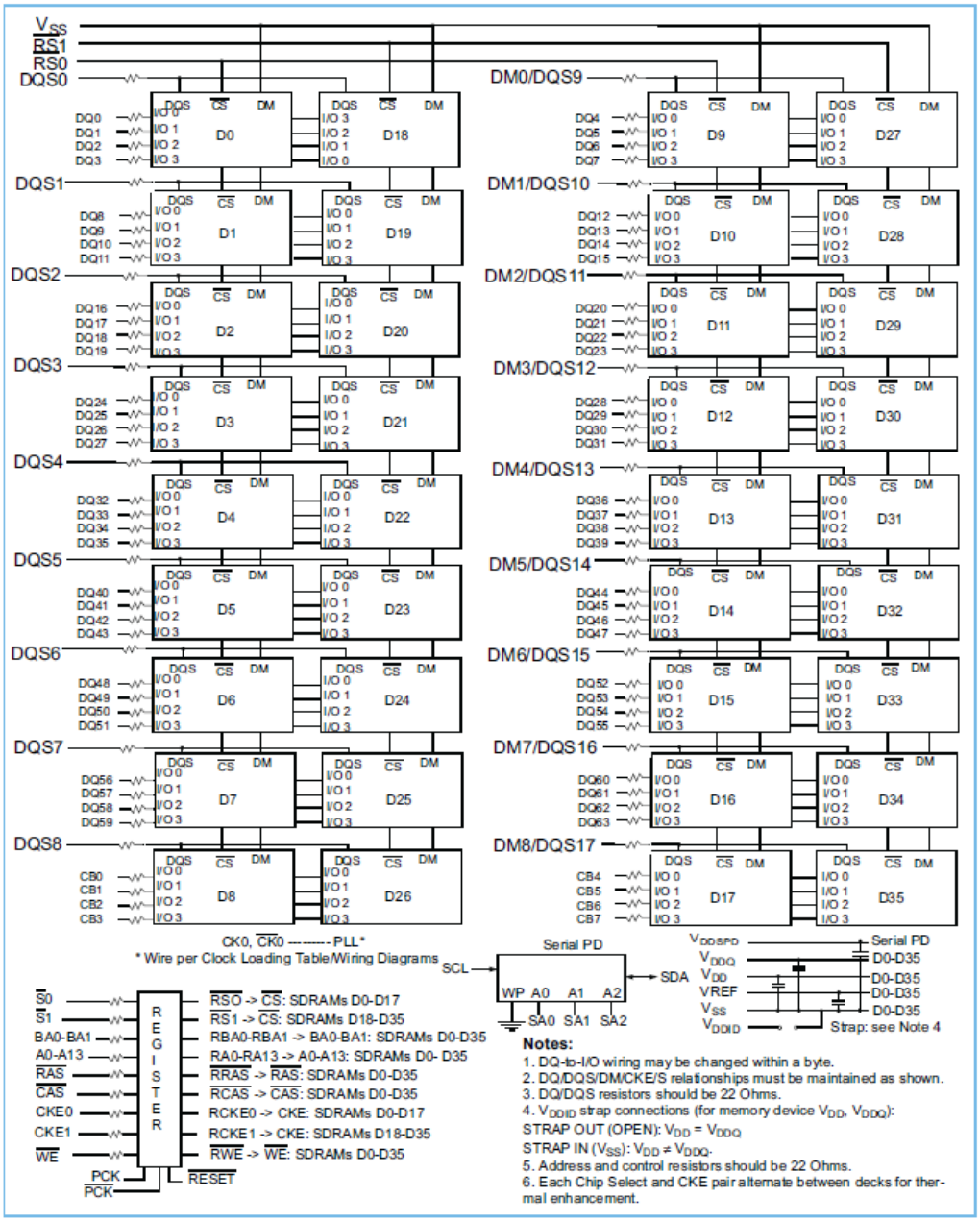


Fig. 4

Halbert, Fig. 4; Decl., ¶¶ 182, 186.

To the extent Halbert does not teach this limitation, it would have been obvious in view of JESD21-C. JESD21-C discloses a first and second set of registered input chip select signals RS0 and RS1 output from the register, as shown in Card N below. RS0 and RS1 correspond to the first and second plurality of input chip select signals S0 and S1 and are shown as input to each bank of memory ranks. Registered chip select RS0 corresponds to the D0-D17 memory ranks, and registered chip select RS1 corresponds to the D18-D35 memory ranks.

Block Diagram: Raw Card Version N (Populated as two physical banks of x4 DDR SDRAMs)



JESD21-C, 15; Decl., ¶¶ 183, 187. JESD21-C's Card N discloses a block diagram of two physical banks of x4 DDR SDRAMs, which is what is disclosed in Fig. 4 of Halbert, i.e., memory device ranks 140 and 142. Thus, like Fig. 2 in Halbert, there would be a first and second plurality of registered chip selects output from module

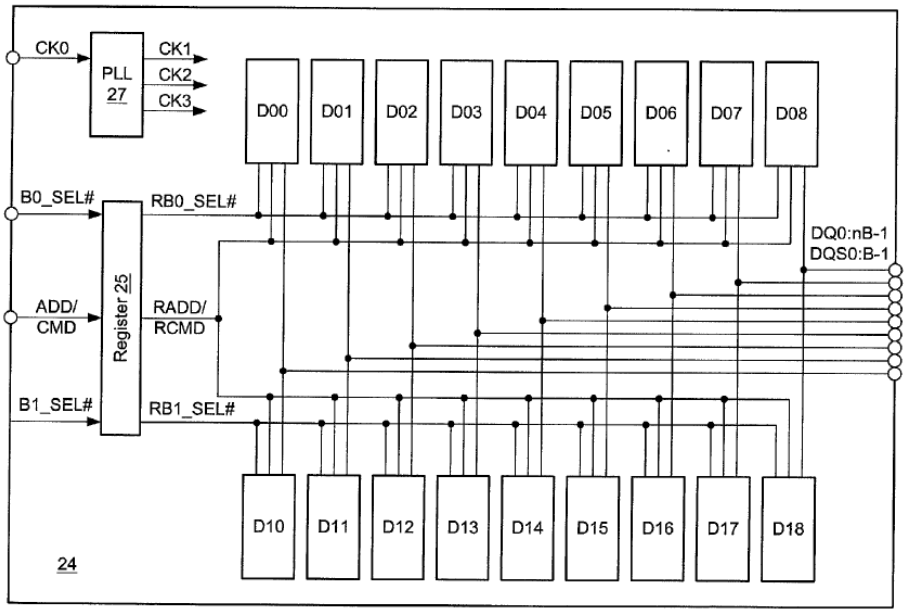
controller 110 in Fig. 4 that correspond to the first and second plurality of input chip select signals. *Id*..

A POSITA would have been motivated to combine the teachings of JESD21-C with Halbert for at least the reasons specified above. *See* §V.C.1.b; Decl., ¶¶ 184, 188.

d. Limitations [3.7]-[3.8]

Halbert discloses Limitations [3.7]-[3.8]. As discussed above, Halbert discloses first and second sets of registered chip select signals RB0_SEL# and RB1_SEL#. Referring to Fig. 2 below, RB0_SEL# has an active signal value when selecting the D00-D08 memory ranks for data transfers. When RB0_SEL# has an active signal value, RB1_SEL# has a non-active signal value because the D10-D18 memory ranks are not selected for data transfers. The opposite happens when D10-D18 memory ranks are selected for data transfers (RB1_SEL# has an active signal value), and D00-D08 memory ranks are not selected for data transfers (RB0_SEL# has a non-active signal value).

Fig. 2
(Prior Art)



Halbert, Fig. 2; Decl., ¶¶ 189, 191.

RB0_SEL# having an active signal value while RB1_SEL# has a non-active signal value is reflected in Fig. 3 below.

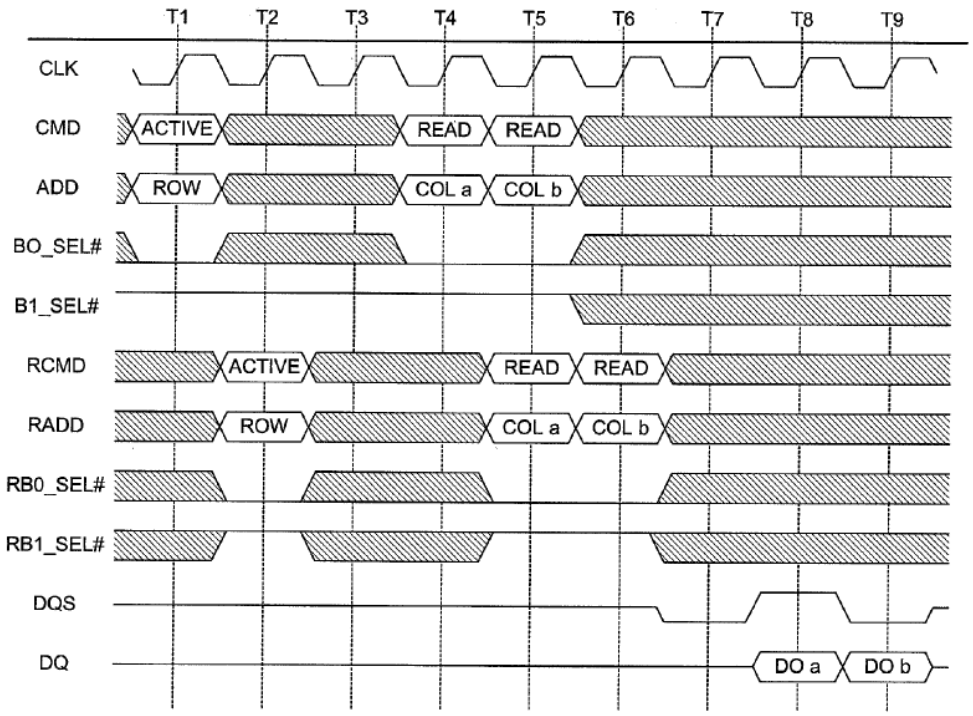


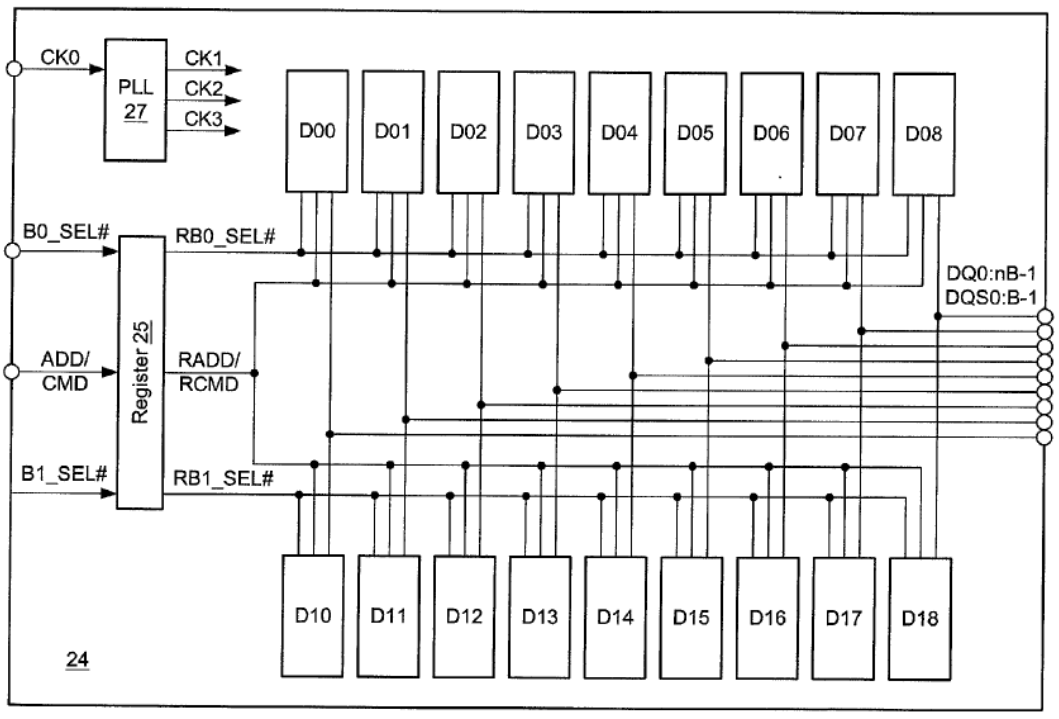
Fig. 3
(Prior Art)

Halbert, Fig. 3. As shown in Fig. 3, RB0_SEL# is low to indicate that it has an active signal value at all times the registered address and control signals are active, while RB1_SEL# is high to indicate that it has a non-active signal value during those times. Decl., ¶ 190. Further, while Fig. 3 is the timing diagram for two consecutive read operations, the RB1_SEL# and RB0_SEL# operate in the same manner for the write operation. Decl., ¶ 192. For the write operation, the signal for RB0_SEL# in Fig. 3 could have the signal for RB1_SEL# instead, and the signal for RB1_SEL# in Fig. 3 could have the signal for RB0_SEL# instead. *Id.* RB1_SEL# would then be low to indicate that it has an active signal value at all times the registered address and control signals are active, while RB0_SEL# would be high to indicate that it has a non-active signal value during those times. *Id.*

e. Limitation [3.9]

Halbert discloses Limitation [3.9]. As discussed above for Limitations [3.5] and [3.6], Halbert discloses that the logic is configured to output first registered chip select signals and second registered chip select signals. The "two bank select signals, B0_SEL# and B1_SEL#, each pass[ing] through register 25 and connect[ing] to a chip select pin on a corresponding one of the banks of memory devices." Halbert, [0009]. Thus, RB0_SEL# can be output to the first rank, i.e., D00-D08, and RB1_SEL# can be output to the second rank, i.e., D10-D18, as shown in Fig. 2 below.

Fig. 2
(Prior Art)



Halbert, Fig. 2. Referring to Fig. 4, a POSITA would have understood that, similar to register 25 in Fig. 2, module controller 110 can output RB0_SEL# to memory rank 140 and RB1_SEL# to memory rank 142. Decl., ¶ 193.

2. Claim 9

a. Limitation [9.1]

Claim 9 depends on claim 1. Halbert discloses Limitation [9.1]. Halbert discloses that "[i]n FIG. 4, R=2, i.e., the memory device array comprises two memory device ranks 140 and 142, each capable of performing m-bit-wide data transfers." Halbert, [0030]. Halbert further discloses that "[t]he types, sizes, or numbers of memory devices selected for use with the present invention are not critical" (*id*., [0061]) and that in memory device banks, "[a] total of nB DQ lines carry data signals, where B is the number of devices in one bank (e.g., eight or nine), and n is the data width of each device (e.g., four, eight, or sixteen bits)" (*id*., [0009]). Thus, Halbert discloses that memory device ranks 140 and 142 could each contain nine devices with eight-bit data widths to provide for 72-bit-wide data transfers. Decl., ¶¶ 195-196.

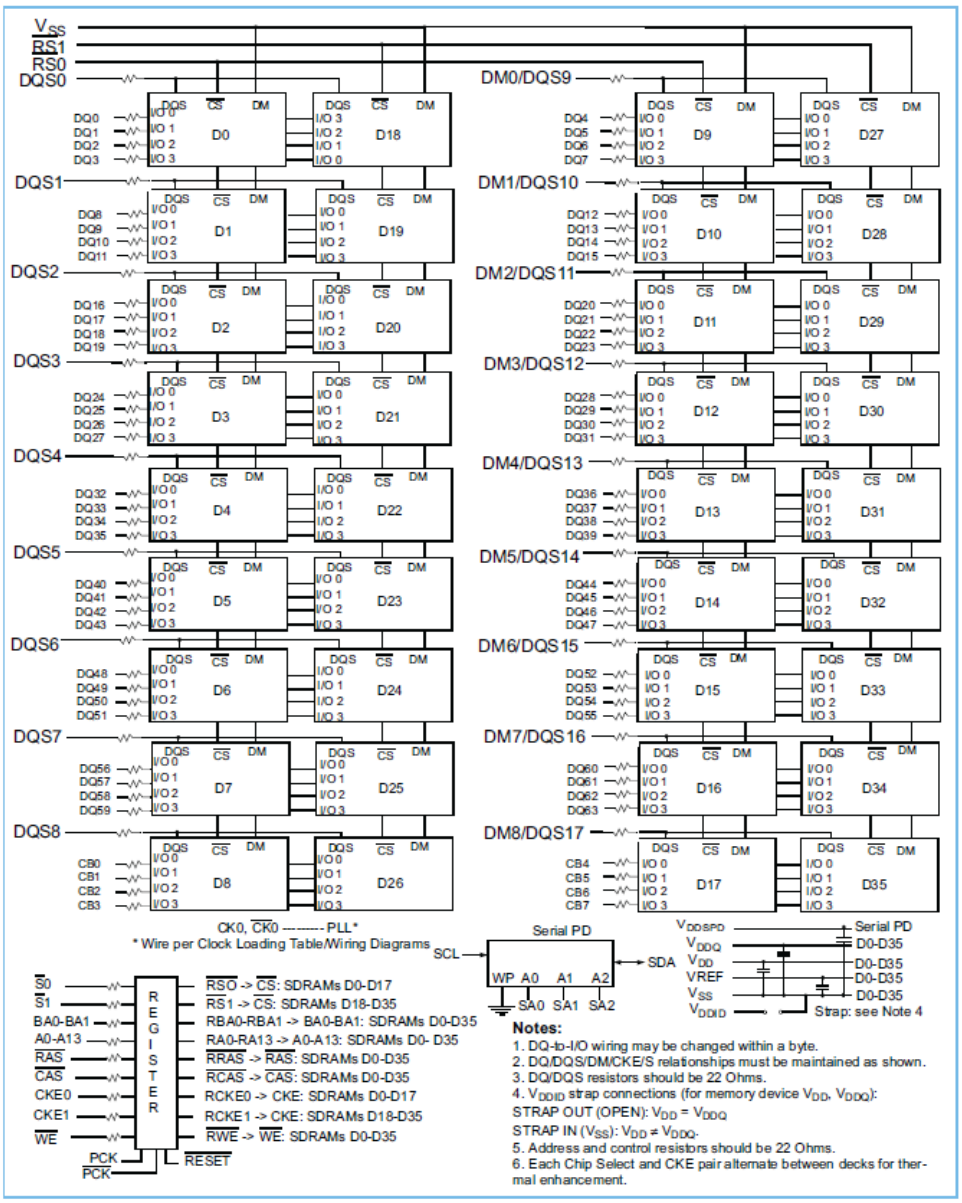
b. Limitation [9.2]

Halbert discloses Limitation [9.2]. Halbert discloses that "[t]he types, sizes, or numbers of memory devices selected for use with the present invention are not critical" (Halbert, [0061]) and that in memory device banks, "[a] total of nB DQ lines carry data signals, where B is the number of devices in one bank (e.g., eight or

nine), and n is the data width of each device (e.g., four, eight, or sixteen bits)" (*id*., [0009]). Thus, it would have been obvious that memory device ranks 140 and 142 could each contain 18 devices configured in 9 pairs with four-bit data widths to provide for 72-bit-wide data transfers. Decl., ¶ 197.

To the extent Halbert does not teach this limitation, it would have been obvious in view of JESD21-C. As shown in Card N below, JESD21-C discloses two physical banks of x4 DDR SDRAMs.

Block Diagram: Raw Card Version N (Populated as two physical banks of x4 DDR SDRAMs)



JESD21-C, 15. The first physical bank of x4 DDR SDRAM has 18 memory integrated circuits, e.g., D0-D17, each 4-bits wide, e.g., I/O0-I/O3, arranged in 9 pairs, e.g., DQ0-DQ3 on D0 and DQ4-DQ7 on D9, DQ8-DQ11 on D1 and DQ12-DQ15 on D10, etc. Likewise, Card N discloses a second physical bank of x4 DDR SDRAM that has 18 memory integrated circuits, e.g., D18-D35, each 4-bits wide,

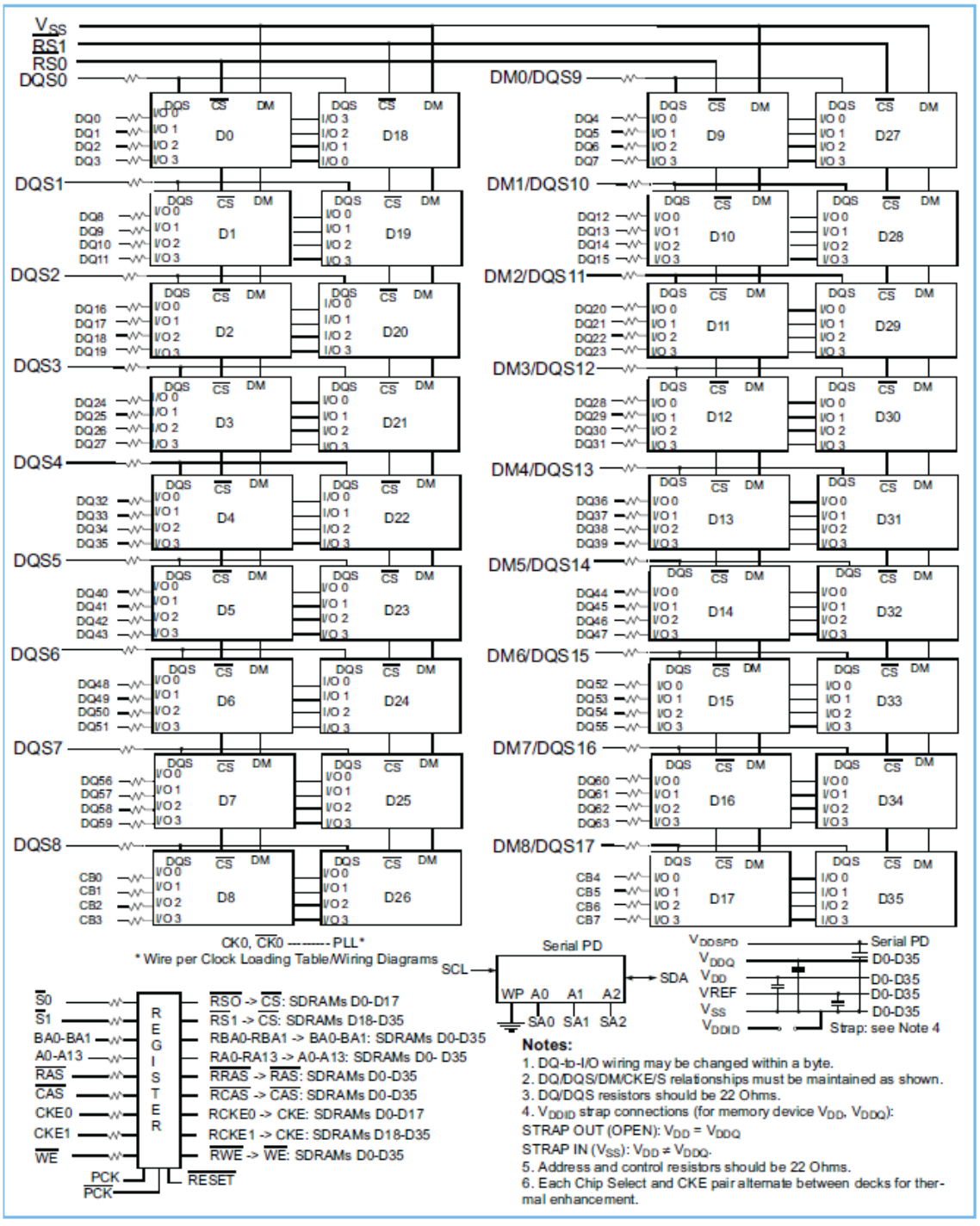
e.g., I/O0-I/O3, arranged in 9 pairs, e.g., DQ0-DQ3 on D18 and DQ4-DQ7 on D27, DQ8-DQ11 on D19 and DQ12-DQ15 on D28, etc. Thus, JESD21-C discloses a plurality of N-bit wide ranks that includes 18 4-bit wide memory integrated circuits configured in 9 pairs. Decl., ¶ 198.

A POSITA would have been motivated to combine the teachings of JESD21-C with Halbert for at least the reasons specified above. *See* §V.C.1.b; Decl., ¶ 199.

c. Limitations [9.3]-[9.4]

Halbert in view of JESD21-C would have rendered Limitations [9.3]-[9.4] obvious. As discussed above for limitation [9.2], JESD21-C discloses in Card N below that each rank of the plurality of N-bit wide ranks includes eighteen 4-bit wide memory integrated circuits configured in nine pairs. D0 and D9 are a first pair of memory integrated circuits that communicate on DQ0-DQ3 and DQ4-DQ7, respectively, providing a total of 8 bits, i.e., a byte, of the 72-bit wide memory rank, i.e., D0-D17. D18 and D27 are a second pair of memory integrated circuits that communicate on DQ0-DQ3 and DQ4-DQ7, respectively, providing a total of 8 bits, i.e., a byte, of the 72-bit wide memory rank, i.e., D18-D35. Decl., ¶¶ 200, 202; *see also id*., [0009] ("n is the data width of each device (e.g., four … bits)."). Moreover, as discussed above for Limitations [12.1] and [12.2], Halbert discloses that first and second bursts of N-bit wide data signals are communicated in each time interval of a first and second plurality of time intervals.

Block Diagram: Raw Card Version N (Populated as two physical banks of x4 DDR SDRAMs)



JESD21-C, 15; Decl., ¶¶ 200, 202.

A POSITA would have been motivated to combine the teachings of JESD21-C with Halbert for at least the reasons specified above. *See* §V.C.1.b; Decl., ¶¶ 201, 203.

3. Claim 10

a. Limitations [10.1]-[10.2]

Claim 10 depends on claim 9. Halbert in view of JESD21-C would have rendered Limitations [10.1]-[10.2] obvious. As discussed above for Limitations [9.3]-[9.4], JESD21-C discloses a first and second pair of memory integrated circuits, configured to communicate a total of eight bits, respectively. Accordingly, a POSITA would have understood that the first and second pair of memory integrated circuits are configured to simulate an 8-bit wide memory device because they communicate using 8-bit wide data transfers. Decl., ¶¶ 205-206, 208.

A POSITA would have been motivated to combine the teachings of JESD21-C with Halbert for at least the reasons specified above. *See* §V.C.1.b; Decl., ¶¶ 207, 209.

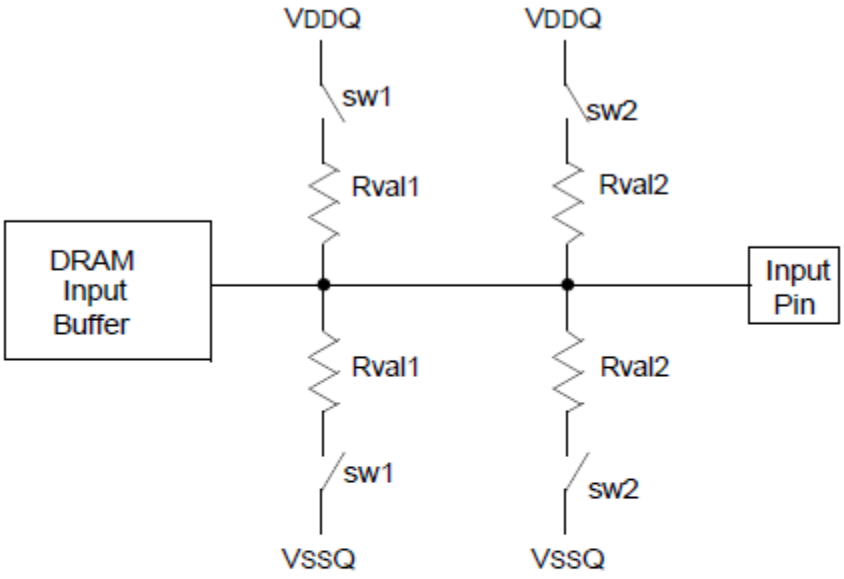
D. Ground 3: Halbert in View of JESD79-2A Render Claim 5 Obvious

1. Claim 5

a. Limitation [5.1]

Claim 5 depends on claim 1. Halbert in view of JESD79-2A would have rendered Limitation [5.1] obvious. JESD79-2A discloses the use of on die

termination in a DRAM memory device. "On Die Termination (ODT) is a feature that allows a DRAM to turn on/off termination resistance for each DQ, DQS/DQS, RDQS/RDQS, and DM signal for x4x8 configurations via the ODT control pin. For x16 configuration ODT is applied to each DQ, UDQS/UDQS, LDQS/LDQS, UDM, and LDM signal via the ODT control pin." JESD79-2A, 26. The functional representation of an ODT circuit is shown in Fig. 15 below.



Switch sw1 or sw2 is enabled by ODT pin.
Selection between sw1 or sw2 is determined by "Rtt (nominal)" in EMRS
Termination included on all DQs, DM, DQS, $\overline{\text{DQS}}$, RDQS, and $\overline{\text{RDQS}}$ pins.
Target Rtt (ohm) = (Rval1) / 2 or (Rval2) / 2

Figure 15 — Functional Representation of ODT

Id., Fig. 15; Decl., ¶¶ 212-213.

It would have been obvious to a POSITA for the ODT circuit in Fig. 15 of JESD79-2A to be included as part of Halbert's memory module 100 shown in Fig.

4, such that memory module 100 is configured to receive from memory controller 20 an ODT signal at an ODT control pin. Decl., ¶ 214. As disclosed in JESD79-2A, "[t]he ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to independently turn on/off termination resistance for any or all DRAM devices." JESD79-2A, 26. Thus, it would have been obvious to include the ODT circuit in memory module 100 to improve the signal integrity of memory module 100. Decl., ¶ 214.

Furthermore, a POSITA would have been motivated to combine the teachings of Halbert with JESD79-2A because both references are in the same field, directed toward solving the same problem, i.e., improving DDR SDRAM design. Decl., ¶ 215. More specifically, a POSITA would have been motivated to design DDR SDRAMs, such as those disclosed in Halbert, to be in compliance with an industry-wide governing standard such as JEDEC. *Id*. A POSITA would have understood that modifying Halbert's memory module 100 shown in Fig. 4 with the teachings of JESD79-2A would have been obvious because Halbert is directed to "memory module configurations and access methods … [that] can improve on the dual-bank registered DIMM in several respects" (Halbert, [0024]), and JESD79-2A is directed to facilitating interchangeability and improvement of DDR2 SDRAM products (JESD79-2A, 2). Decl., ¶ 215. Thus, both references are directed to achieving the same goal, and a POSITA would have been motivated to incorporate any additional

standardized DDR SDRAM design requirements into Halbert's memory module 100. *Id*.

Moreover, JESD79-2A is a specification for defining several aspects of 64 Mb through 1 Gb DDR2 SDRAMs with x4/x8/x16 data interfaces. JESD79-2A, 15-16; Decl., ¶ 216. This is the exact type of memory device that is disclosed in Halbert. "Some possible device types include dynamic random access memory (DRAM) devices, synchronous DRAM (SDRAM) devices including double-data-rate (DDR) SDRAM devices." Halbert, [0061]; Decl., ¶ 216. And the basic operation of memory module 100 of Halbert is the same as the functionality of DDR2 SDRAM described in JESD79-2A. *See, e.g.*, Halbert, 37 ("When controller 110 latches an active command into RCMD, it enters an ACTIVE state itself. In the ACTIVE state, controller 110 scans the command bus for READ or WRITE commands.") and JESD79-2A, 18 ("Read and write accesses to the DDR2 SDRAM are burst oriented; … Accesses begin with the registration of an Active command, which is then followed by a Read or Write command."); Decl., ¶ 216.

Applying the teachings of JESD79-2A to Halbert would not have been beyond the skill of a POSITA and would follow the typical course of technological progression. Decl. ¶ 217. A POSITA would have understood that whether to include ODT functionality in memory modules is a design choice. *Id*. Accordingly, modifying Halbert's memory module 100 to incorporate the ODT functionality

disclosed in the contemporaneous JESD79-2A would have been obvious. *Id*. Such a modification would also have been obvious because it was a one of a finite number of solutions, not beyond the skill of an ordinary artisan to implement, and would have yielded predictable results. *Id*. Thus, a POSITA would have been motivated to incorporate the teachings of JESD79-2A into the memory system of Halbert. *Id*.

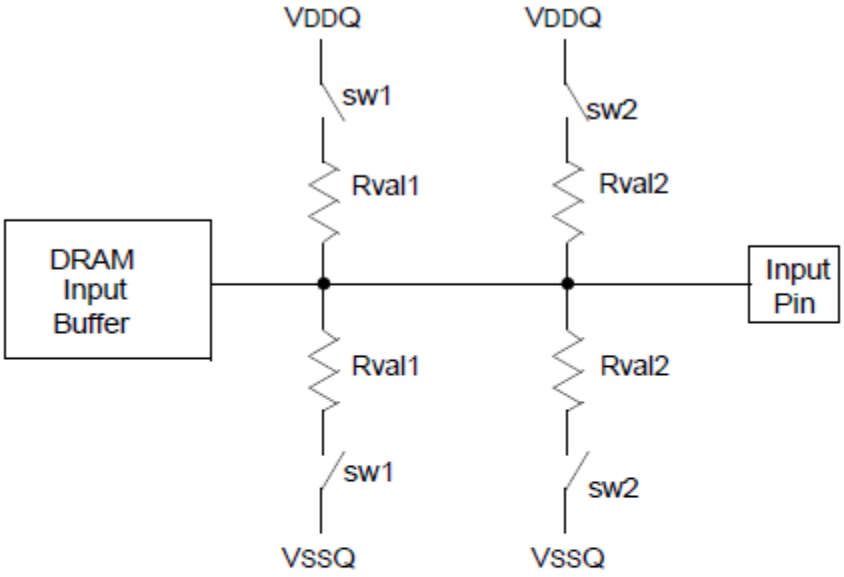
b. Limitation [5.2]

Halbert in view of JESD79-2A would have rendered Limitation [5.2] obvious. JESD79-2A discloses that on die "[t]ermination [is] included on all DQs, DM, DQS, DQS [bar], RDQS, and RDQS [bar] pins." JESD79-2A, Fig. 15. A POSITA would have understood that for termination to be included on all DQs, i.e., data lines, each of the plurality of memory integrated circuits, i.e., memory devices of memory ranks 140 and 142, would include an ODT circuit. Decl., ¶ 218. As disclosed in JESD79-2A, "[t]he ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to *independently turn on/off termination resistance for any or all DRAM devices*." JESD79-2A, 26 (emphasis added); *see also id*., 14 ("On Die Termination: ODT (registered HIGH) enables termination resistance internal to the DDR2 SDRAM."). Thus, it would have been obvious to include an ODT circuit for each memory device of memory ranks 140 and 142 because an ODT circuit on each memory device helps the memory ranks minimize signal noise and improve signal integrity. Decl., ¶ 218.

A POSITA would have been motivated to combine the teachings of JESD79-2A with Halbert for at least the reasons specified above. *See* §V.D.1.a; Decl., ¶ 219.

c. Limitation [5.3]

Halbert in view of JESD79-2A would have rendered Limitation [5.3] obvious. Turning on/off termination resistance is done via the ODT control pin. *Id.* A functional representation of an ODT circuit is shown in Fig. 15 below.



Switch sw1 or sw2 is enabled by ODT pin.
Selection between sw1 or sw2 is determined by "Rtt (nominal)" in EMRS
Termination included on all DQs, DM, DQS, $\overline{\text{DQS}}$, RDQS, and $\overline{\text{RDQS}}$ pins.
Target Rtt (ohm) = (Rval1) / 2 or (Rval2) / 2

Figure 15 — Functional Representation of ODT

Id.; Decl., ¶ 220.

JESD79-2A discloses the functionality of an ODT circuit in a memory device but does not require any specific implementation of ODT circuits, which are simply used for termination, in memory modules. Indeed, "[t]he ODT feature is designed to improve signal integrity of the memory channel by *allowing the DRAM controller to independently turn on/off termination resistance for any or all DRAM devices*." JESD79-2A, 26 (emphasis added). Thus, it would have been obvious to a POSITA to also include a termination circuit external to memory ranks 140 and 142 to allow for more termination options to "turn on/off termination resistance for any or all DRAM devices." *Id.*; Decl., ¶ 221. For example, a termination circuit could be included outside memory rank 142 that is connected to RDQ1. Decl., ¶ 221. The memory module's signals can then be terminated at "any or all DRAM devices" of each memory rank or on the overall memory module 100's circuit board, which allows for more precision in the memory module design, provides for more termination resistor options, and allows for improved signal integrity to come into the memory module or the plurality of memory integrated circuits. *Id.*

A POSITA would have been motivated to combine the teachings of JESD79-2A with Halbert for at least the reasons specified above. *See* §V.D.1.a; Decl., ¶ 222.

d. Limitation [5.4]

Halbert in view of JESD79-2A would have rendered Limitation [5.4] obvious. As discussed above for Limitation [5.3], it would have been obvious to include a

termination circuit on memory module 100 that is external to each of memory ranks 140 and 142. JESD79-2A discloses that ODT "is a feature that allows a DRAM to turn on/off termination resistance for each DQ, DQS/DQS, RDQS/RDQS, and DM signal for x4x8 configurations via the ODT control pin. For x16 configuration ODT is applied to each DQ, UDQS/UDQS, LDQS/LDQS, UDM, and LDM signal via the ODT control pin." JESD79-2A, 26. Thus, it would have been obvious to a POSITA that in order for the memory module to turn on/off the termination resistance for any or all DRAM devices of memory ranks 140/142, the termination circuit external to the memory devices of the memory ranks would be configured to receive the ODT signal and be coupled to the ODT circuit of at least one of the DRAM devices of memory ranks 140/142 to be able to pass the ODT signal to the ODT circuit of at least one of the DRAM devices of memory device ranks 140/142. Decl., ¶ 223. As discussed above, with this configuration, the memory module's signals can then be terminated at each memory rank or on the overall memory module 100's circuit board, which allows for more precision in the memory module design, provides for more termination resistor options, and improves signal integrity. *Id*.

A POSITA would have been motivated to combine the teachings of JESD79-2A with Halbert for at least the reasons specified above. *See* §V.D.1.a; Decl., ¶ 224.

e. Limitation [5.5]

Halbert in view of JESD79-2A would have rendered Limitation [5.5] obvious. As discussed above for Limitation [5.4], it would have been obvious for the termination circuit that is external to memory ranks 140/142 to be configured to receive the ODT signal and pass the ODT signal to the ODT circuit of at least one of the memory devices of memory ranks 140/142. JESD79-2A discloses that ODT "is a feature that allows a DRAM to turn on/off termination resistance for each DQ, DQS/DQS, RDQS/RDQS, and DM signal for x4x8 configurations via the ODT control pin. For x16 configuration ODT is applied to each DQ, UDQS/UDQS, LDQS/LDQS, UDM, and LDM signal via the ODT control pin." JESD79-2A, 26. Thus, it would have been obvious to a POSITA that if the termination circuit is coupled to the ODT circuit of at least one of the memory devices of memory ranks 140/142, then the termination circuit can provide external termination for at least one memory device of the memory ranks 140/142 it is coupled to in response to the ODT signal because the termination resistance of the coupled memory rank can be off while the termination resistance of the termination circuit can be on, and in this configuration, the ODT signal would provide external termination for the coupled memory rank. Decl., ¶ 225.

Moreover, JESD79-2A discloses that "[t]he ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller

to *independently turn on/off termination resistance for any or all DRAM devices*." JESD79-2A, 26 (emphasis added). Therefore, as discussed above, with this configuration, the memory module's signals can then be terminated at each memory device or on the overall memory module 100's circuit board, which allows for more precision in the memory module design and provides for more termination resistor options. Decl., ¶ 226.

A POSITA would have been motivated to combine the teachings of JESD79-2A with Halbert for at least the reasons specified above. *See* §V.D.1.a; Decl., ¶ 227.

f. Limitation [5.6]

Halbert in view of JESD79-2A would have rendered Limitation [5.6] obvious. It would have been obvious to a POSITA that for the termination circuit that is coupled to the ODT circuit of at least one memory device of memory ranks 140/142 to provide external termination for the memory device it is coupled to, in response to the ODT signal, the termination resistance of the coupled memory device would have to be off while the termination resistance of the termination circuit is on. Decl., ¶ 228. This is because if the termination resistances are enabled at both the ODT of the coupled memory device and the termination circuit, the termination resistance will be cut in half, creating a mismatch, and a shared signal to the coupled memory device would not be properly terminated. *Id*. Thus, in this external termination configuration, the ODT circuit of the coupled memory rank is disabled. *Id*.

A POSITA would have been motivated to combine the teachings of JESD79-2A with Halbert for at least the reasons specified above. *See* §V.D.1.a; Decl., ¶ 230.

E. No Secondary Considerations Exist

The combinations of Halbert in view of a POSITA's knowledge, Halbert in view of JESD21-C, and Halbert in view of JESD79-2A would have rendered the Challenged Claims of the '314 patent obvious. No secondary indicia of non-obviousness having a nexus to the putative "invention" of these claims exists contrary to that conclusion. Petitioners reserve their right to respond to any assertion of secondary indicia of nonobviousness advanced by Patent Owner.

VI. The Parallel District Court Case Does Not Warrant Denying Institution

When considering a parallel proceeding, the PTAB "balance[s] considerations such as system efficiency, fairness, and patent quality" using the six factors set forth by the Board in *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 at 5 (PTAB Mar. 20, 2020) (precedential). These factors "overlap," and a "holistic view" should be taken. *Id.,* 6.

The fourth factor (overlap) strongly favors institution. Petitioners have stipulated that they will not pursue invalidity on the same grounds—or even the same references—if the Board institutes trial in this proceeding. Ex. 1010. Petitioners modeled this stipulation on one the Board found to "mitigate any concerns" in *VMware, Inc. v. Intellectual Ventures I LLC*, IPR2020- 00470, Paper

13 at 20 (P.T.A.B. August 18, 2020). This fourth factor favors institution here even more so than in *Apple, Inc. v. SEVEN Networks, LLC*, IPR2020-00156, Paper 10 (P.T.A.B. June 15, 2020). There, the petitioner provided no stipulation. *Id*., 16-19. Nevertheless, the fourth factor "strongly favored" petitioner. *Id*.

The third factor (investment in parallel proceeding) also favors institution. The district court has not issued any substantive opinions regarding the scope or validity of the Challenged Claims, and given Petitioners' stipulations, the Court is unlikely to invest any resources on the grounds raised in this Petition, either before or after the scheduled institution date. Furthermore, the parallel proceeding is in an early stage, fact discovery has not yet opened, and no trial date has been set. Only initial contentions and claim construction briefs have been exchanged. Ex. 1011.

Regarding the sixth factor (merits, other circumstances), the merits strongly weigh in favor of instituting trial as shown through the strength of the grounds in this Petition. Other circumstances also favor institution. Like in *Apple v. SEVEN*, the parallel litigation is complex, involving substantial litigation and IPR history regarding the family of patents associated with the '314 patent, three patents, 37 asserted claims, and many accused products. *SEVEN*, 21-22. An IPR trial, in contrast, allows a focus on resolving all Challenged Claims in a single patent, thus "enhanc[ing] the integrity of the patent system." *SEVEN*, 22.

Fintiv factors 1 (stay) and 2 (proximity of trial dates) favor institution. The Court has not yet set the trial date and the related litigation is currently stayed other than claim construction. With the case currently stayed, the Board should consider these two factors "weigh[ing] strongly against exercising [PTAB's] discretion to deny institution." *Shure Inc. v. Clearone, Inc.*, PGR2020-00079, Paper 14 at 15–16, (February 16, 2021) ("In any case, unlike in the NHK and Fintiv cases, there is no trial date set in the Illinois case. Thus, this factor weighs strongly against exercising our discretion to deny the Petition.").

For these reasons, the Board should not exercise its discretion to deny institution of this Petition.

VII. Discretionary Denial Under § 325(d) Is Not Warranted

Advanced Bionics and § 325(d) do not support discretionary denial. The Board's precedential decision in *Advanced Bionics* establishes a two-part framework for evaluating discretionary denial under § 325(d). *Advanced Bionics, LLC v. MED-EL Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6, 8 (PTAB Feb. 13, 2020) (precedential).[4]

[4] The Board noted that the six *Becton, Dickinson* factors a-f are helpful in guiding the two-pronged analysis under *Advanced Bionics*, with factors a, b, and d relevant

As to the first prong, although Halbert and JESD21-C were identified on IDS's, JESD79-2A was not previously presented to the Office. For at least this reason—the first prong weighs in favor of institution.

As to the second prong, the Examiner "erred in a manner material to the patentability of challenged claims" by overlooking the relevance of Halbert, JESD21-C, and JESD79-2A (the "Asserted Art") against the Challenged Claims of the '314 patent, as shown below. *Advanced Bionics*, IPR2019-01469, Paper 6, 8.

Becton, Dickinson factor c favors institution. The "extent to which the asserted art was evaluated during examination" is nil because the Examiner did not issue a single rejection, much less one where the Asserted Art "was the basis for rejection." *Id.*, 9 n.10. Rather than issuing even a single rejection, the first action on the merits by the Examiner was a Notice of Allowance. Ex. 1002, 210. And even there, the Examiner failed to mention or comment on the Asserted Art—even at a cursory level. *Id.*

Becton, Dickinson factor e favors institution. As shown in the grounds of this Petition, the Asserted Art renders the Challenged Claims obvious. Yet, as noted above, the Examiner never commented on the Asserted Art's relevance, much less

---

to the first prong of the *Advanced Bionics* framework, and factors c, e, and f relevant to the second prong. *Advanced Bionics*, IPR2019-01469, Paper 6, 9-11.

issue a rejection based on them. As such, the Examiner clearly overlooked their relevance. Such human error/oversight in overlooking their relevance is understandable since Patent Owner submitted hundreds of references in numerous IDS's to the Office. Ex. 1002, 164-203. Nonetheless, the Board in *Advanced Bionics* made clear that even such oversight is still one clear example of material error that would preclude discretionary denial under § 325(d). *Advanced Bionics*, IPR2019-01469, Paper 6, 8 n.9 ("An example of a material error may include . . . overlooking specific teachings of the relevant prior art where those teachings impact patentability of the challenged claims"); *id.*, 10 ("[I]f the record of the Office's previous consideration of the art is not well developed or ***silent***, then a petitioner may show the Office erred by overlooking something persuasive under factors (e) and (f)."") (emphasis added).

The Examiner's material error—overlooking specific teachings of relevant prior art—is even more evident considering that the Board in IPR2017-00549 relied upon Halbert to find challenged claims in a patent in the '314 patent's extended family unpatentable, and the Board in IPR2014-00883, IPR2015-01021, and IPR2015-01020 relied upon JESD21-C to find claims in the '314 patent's extended family unpatentable. *See supra*, § III(D). Thus, what is clear is that when Halbert and JESD21-C have been substantively considered when evaluating the patentability of patents in the '314 patent's extended family, the result is claims have been found

unpatentable. As shown in the grounds of this Petition, the Challenged Claims are unpatentable. Considering the foregoing, the Examiner made a material error during prosecution that warrants institution.

Becton, Dickinson factor f favors institution. This Petition presents, along with the Asserted Art, the declaration of Dr. Oklobdzija that elaborates on how the teachings of the Asserted Art renders obvious the Challenged Claims. Petitioner submits that the Patent Office would have found the Challenged Claims unpatentable as obvious over the Asserted Art had Dr. Oklobdzija's declaration also been before the Office during prosecution.

As shown, the Asserted Art renders the Challenged Claims unpatentable as obvious, and the strength of the Petition alone supports the Board not exercising its discretion under § 325(d). *See, e.g.*, *Apple, Inc. v. Omni MedSci, Inc.*, IPR2020-00029, Paper 7, 8 (P.T.A.B. Apr. 22, 2020) (finding that "reasonable minds cannot disagree that the Office erred in a manner material to patentability in its treatment of the art by failing to reject the claims … over the references cited in Petitioner's challenges."). The Examiner's material error, detailed above, cements Petitioner's position that discretionary denial of institution under § 325(d) is not warranted. *Advanced Bionics*, IPR2019-01469, Paper 6, 8 n.9.

For at least the foregoing reasons, discretionary denial of institution under § 325(d) is not warranted.

VIII. Mandatory Notices

A. Real Parties-in-Interest

The named Petitioners are the only entities who are funding and controlling this Petition and are therefore all named as real parties-in-interest. No other entity is funding, controlling, or otherwise has an opportunity to control or direct this Petition or Petitioners' participation in any resulting IPR.

B. Related Proceedings

Netlist originally asserted the '314 patent against Petitioners in the Western District of Texas (Waco Division), Case No. 6:21-cv-00431. The case has been transferred to the Western District of Texas (Austin Division), Case No. 1:22-cv-00136-LY.

Petitioners have concurrently filed a second petition challenging different claims of the '314 patent that Netlist has asserted against Petitioners. This Petition challenges claims 1-3, 5-6, 8-10, and 12-14, and IPR2022-00745 challenges claims 15-20 and 22-33.

C. Lead and Backup Counsel

Petitioners' lead and backup counsel are:

Lead Counsel for Petitioner	Backup Counsel for Petitioner
Juan C. Yaquian Winston & Strawn LLP 800 Capital Street, Suite 2400 Houston, TX 77002-2925 JYaquian@winston.com T: 713.651.2600, F: 713.651.2700	Michael Rueckheim Winston & Strawn LLP 255 Shoreline Dr., Suite 520 Redwood City, CA 94065 mrueckheim@winston.com

Lead Counsel for Petitioner	Backup Counsel for Petitioner
USPTO Reg. No. 70,755	T: 650.858.6500, F: 650.858.6550 (*pro hac vice* to be filed) James C. Lin Winston & Strawn LLP 255 Shoreline Dr., Suite 520 Redwood City, CA 94065 jalin@winston.com T: 650.858.6500, F: 650.858.6550 (*pro hac vice* to be filed)

D. Electronic Service

Petitioners consent to electronic service at:

Winston-IPR-NetList@winston.com

IX. Fees

The required fee is being paid electronically through PTAB E2E.

X. Conclusion

Petitioners respectfully request that the Board institute IPR and enter a final written decision finding the Challenged Claims unpatentable.

Dated: March 30, 2022

Respectfully submitted,

/ *Juan C. Yaquian* /
Juan C. Yaquian
Winston & Strawn LLP
800 Capital Street, Suite 2400
Houston, TX 77002-2925
JYaquian@winston.com
T: 713.651.2600, F: 713.651.2700
USPTO Reg. No. 70,755

Lead Counsel for Petitioners

CERTIFICATE OF COMPLIANCE

This Petition complies with the word count limits set forth in 37 C.F.R. § 42.24(a)(1)(i), because this Petition contains 13,995 words, excluding the parts of the Petition exempted by 37 C.F.R. § 42.24(a)(1) and determined using the word count provided by Microsoft Word, which was used to prepare this Petition.

Dated: March 30, 2022

Respectfully submitted,

/ *Juan C. Yaquian* /
Juan C. Yaquian
Winston & Strawn LLP
800 Capital Street, Suite 2400
Houston, TX 77002-2925
JYaquian@winston.com
T: 713.651.2600, F: 713.651.2700
USPTO Reg. No. 70,755

Lead Counsel for Petitioners

CERTIFICATE OF SERVICE

Under 37 C.F.R. §§ 42.6(e) and 42.105(a), this is to certify that on March 30, 2022, I caused to be served a true and correct copy of the foregoing "**PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 10,489,314**" and Exhibits 1001-1011 by Federal Express on the Patent Owner at the correspondence address of record for U.S. Patent No. 10,489,314:

USCH Law, PC
3790 El Camino Real #1147
Palo Alto CA 94304

A courtesy copy of this Petition and supporting material was also served on litigation counsel for Patent Owner via email:

Paul J. Skiermont
SKIERMONT DERBY LLP
pskiermont@skiermontderby.com

/ *Juan C. Yaquian* /
Juan C. Yaquian
Winston & Strawn LLP
800 Capital Street, Suite 2400
Houston, TX 77002-2925
JYaquian@winston.com
T: 713.651.2600, F: 713.651.2700
USPTO Reg. No. 70,755

Lead Counsel for Petitioners